ZYNQ7000 FPGA Development Board AX7Z010

User Manual

ALINX

Version Record

Version	Date	Release By	Description
Rev 1.0	2019-12-15	Rachel Zhou	First Release

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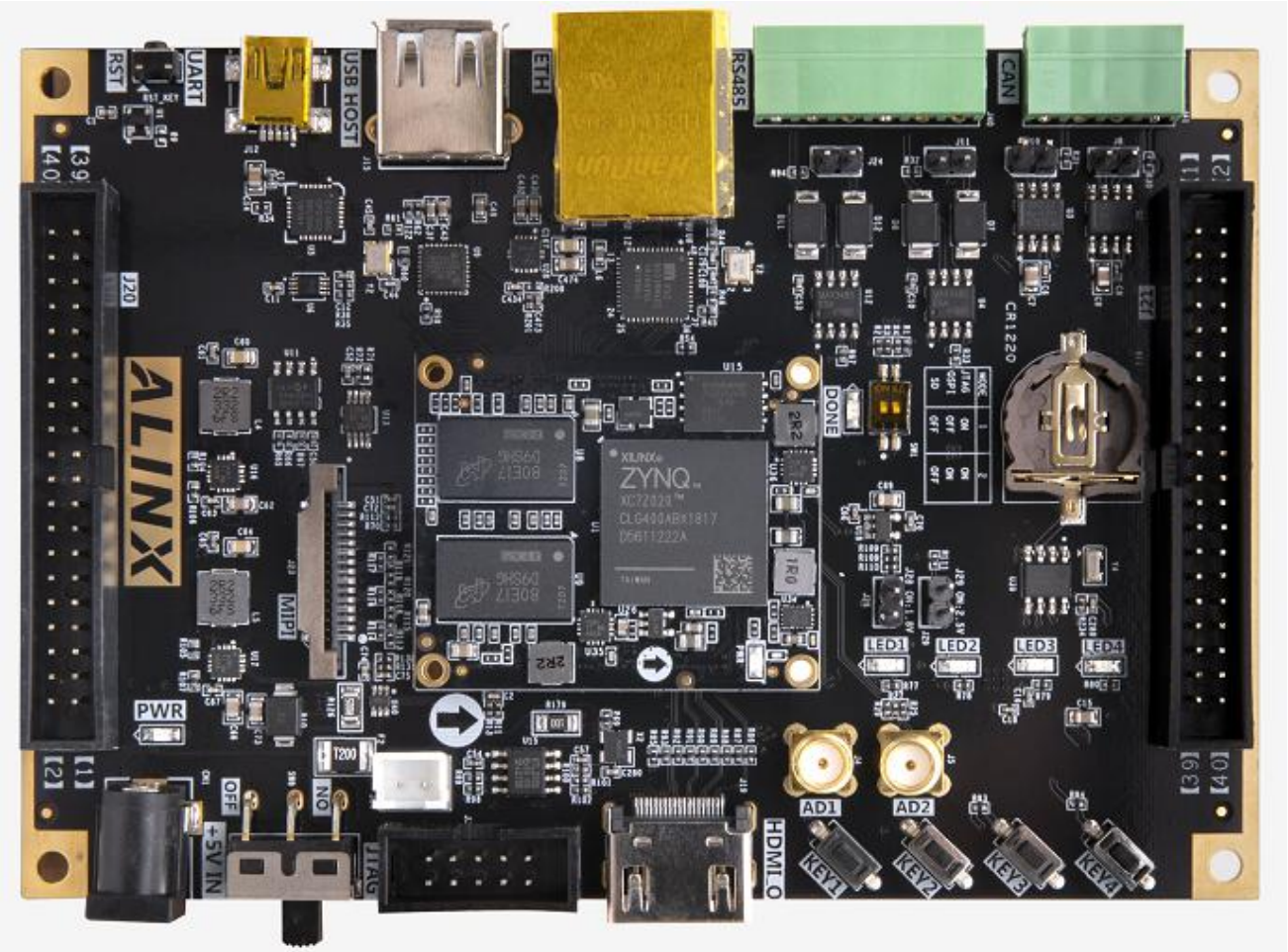
This ZYNQ7000 FPGA development platform adopts the core board + carrier board mode, which is convenient for users to use the core board for secondary development. The core board uses XILINX's Zynq7000 SOC chip XC7Z010 solution, uses ARM+FPGA SOC technology to integrate dual-core ARM Cortex-A9 and FPGA programmable logic on a single chip. In addition, the core board contains 2 pieces of 512MB high-speed DDR3 SDRAM chips, and 1 piece of 256Mb QSPI FLASH chip.

In the design of carrier board, we have extended a wealth of interfaces for users, such as 1 Gigabit Ethernet interfaces, 1 USB2.0 HOST interface, 1 HDMI output interface, 1 UART USB interface. 1 SD card slot, 2-Channel CAN bus interfaces, 2-Channel RS485 bus interfaces, 2-Channel AD input interface, 2-Channel 40-pin expansion header, some keys and LEDs. It meets users' requirements for high-speed Ethernet data exchange, data storage, video transmission processing and industrial control. It is a "professional" ZYNQ development platform. For high-speed data transmission and exchange, pre-verification and post-application of data processing is possible. This product is very suitable for students, engineers and other groups engaged in ZYNQ development.


RST
UART
USB HOST
ETH
RS485
CAN
J20
ZYNQ
DONE
MIPI
PWR
OFF
ON
+5V IN
JTAG
LED1
LED2
LED3
LED4
AD1
AD2
HDMI_O
KEY1
KEY2
KEY3
KEY4
CR1220

Part 1: FPGA Development Board Introduction

The entire structure of the AX7Z010 FPGA development board is inherited from our consistent core board + carrier board model. A high-speed inter-board connector is used between the core board and the carrier board.

The core board is mainly composed of the smallest system of XC7Z010 + 2 DDR3 + QSPI FLASH, which is responsible for the high-speed data processing and storage functions of the ZYNQ system. The data width between the ZYNQ 7010 and the two DDR3 chips is 32 bits. The capacity of two DDR3 chips is up to 512MB. ZYNQ7010 uses Xilinx's Zynq7000 series chip, the model number is XC7Z010-1CLG400I. ZYNQ7010 chip can be divided into processor system part Processor System (PS) and programmable logic part Programmable Logic (PL)

The AX7Z010 carrier board expands its rich peripheral interface, including 1 Gigabit Ethernet interfaces, 1 USB2.0 HOST interface, 1 HDMI output interface, 1 UART USB interface. 1 SD card slot, 2-Channel CAN bus interfaces, 2-Channel RS485 bus interfaces, 2-Channel AD input interface, 2-Channel 40-pin expansion header, some keys and LEDs.

The following figure shows the structure of the entire development system:

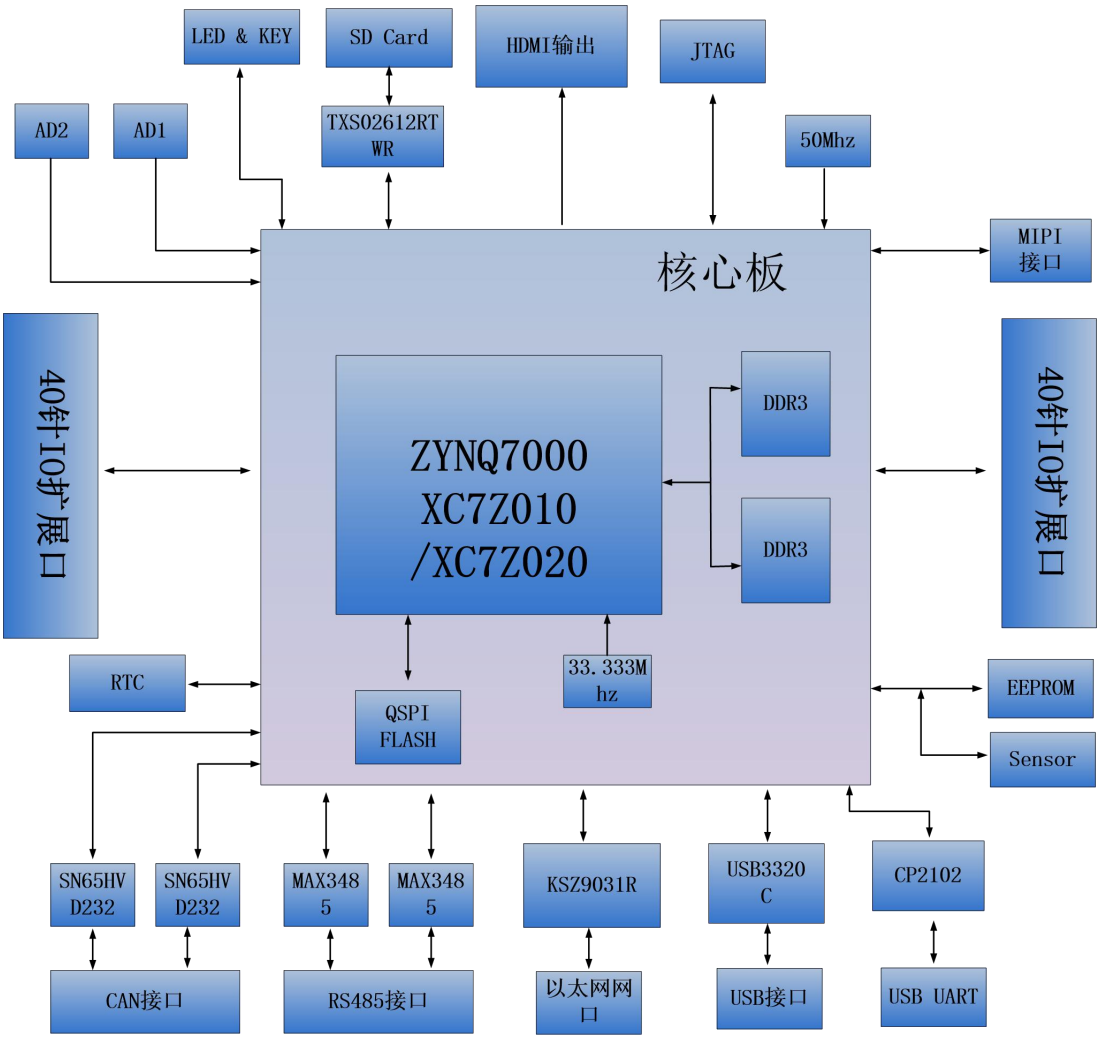


Figure 1-1-1: The Schematic Diagram of the AX7Z010

Through this diagram, you can see the interfaces and functions that the AX7Z010 FPGA Development Board contains:

- ZYNQ7000 core board

  It consists of XC7Z010 + 512MB DDR3 + 256Mb QSPI FLASH, and a 33.333333MHz crystal oscillator provides the clock to the PS system.

- CAN Communication Interface

  2 CAN bus interface, using SN65HVD232 chip from TI Company.

- 485 Communication Interface

  2-Channel 485 communication interfaces, using MAX3485 chip of MAXIM Company.

- Gigabit Ethernet Interface

  1-Channel 10/100M/1000M Ethernet RJ45 interface for Ethernet data exchange with computers or other network devices. The network interface chip uses Micrel's KSZ9031 industrial grade GPHY chip.

- USB 2.0 HOST Interface

  It can be used to connect USB peripherals such as mouse, keyboard and U disk to the development board;

- USB Uart Interface

  1 port Uart to USB interfaces for communication with the computer, for user debugging. The serial port chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface.

- Micro SD card slot

  1-port Micro SD card holder, use to store operating system images and file systems.

- AD analog input interface

  2 AD analog input interfaces, which can be used for analog signal input and voltage conversion, SMA interface form. Analog signal voltage input range is 0 ~ 10V **(Do not input voltage exceeding this range)**

- HDMI video input

  1 channel HDMI image video input interface, can realize 1080P video image transmission.

- EEPROM

  One EEPROM 24LC04 with IIC interface

- Temperature and humidity sensor chip LM75

  On-board temperature and humidity sensor chip LM75, used to detect the temperature and humidity of the surrounding environment around the FPGA development board

- 1 MIPI camera interface

It can be used to connect ALINX OV5640 camera with MIPI interface (**only for AX7Z020**).

- JTAG debug port

  A 10-pin 0.1 spacing standard JTAG ports for FPGA program download and debugging. Users can debug and download the ZYNQ system through the XILINX downloader.

- 40-pin expansion port

  2 40-pin 0.1-inch pitch expansion port can be connected to various ALINX modules (binocular camera, TFT LCD screen, high-speed AD module, etc.). The expansion port contains 1-channel 5V power supply, 2-channel 3.3V power supply, 3-channel way ground, 34 IOs port.

- LED Lights

  7 LEDs, include 6 LEDs on the core board, 1 LED on the carrier board. There is 1 power indicator on the core board, 1 power indicator on the carrier board. There is 1 power indicator, 1 DONE configuration indicator, and 4 user indicators on the carrier board.

- 4 user buttons on the carrier board

Part 2: AC7Z010 core board

Part 2.1: AC7Z010 core board Introduction

AC7Z010 (core board model, the same below) FPGA core board, ZYNQ chip is based on XC7Z010-1CLG400I of XILINX company ZYNQ7000 series. The ZYNQ chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. The FPGA of the ZYNQ chip contains a wealth of programmable logic cells, DSP and internal RAM.

This core board uses two Micron's MT41K128M16TW-107 DDR3 chips, each of which has a capacity of 256MB; the two DDR chips combine to form a 32-bit data bus width, and the clock frequency of read and write data between ZYNQ and DDR3 Up to 533Mhz; this configuration can meet the needs of the system's high-bandwidth data processing

In order to connect with the carrier board, the two board-to-board connectors of this core board are extended with USB ports on the PS side, Gigabit Ethernet interfaces, SD card slot, and other remaining MIO ports (48). As well as almost all IO ports (100) of BANK13 (only for AC7Z010), BAN34 and BANK35 on the PL side, the IO levels of BANK34 and BANK35 can be provided through the carrier board to meet users' requirements for different level interfaces. For users who need a lot of IO, this core board will be a good choice. And the IO connection part, the ZYNQ chip to the interface between the equal length and differential processing, and the core board size is only 35 * 42 (mm), which is very suitable for secondary development.

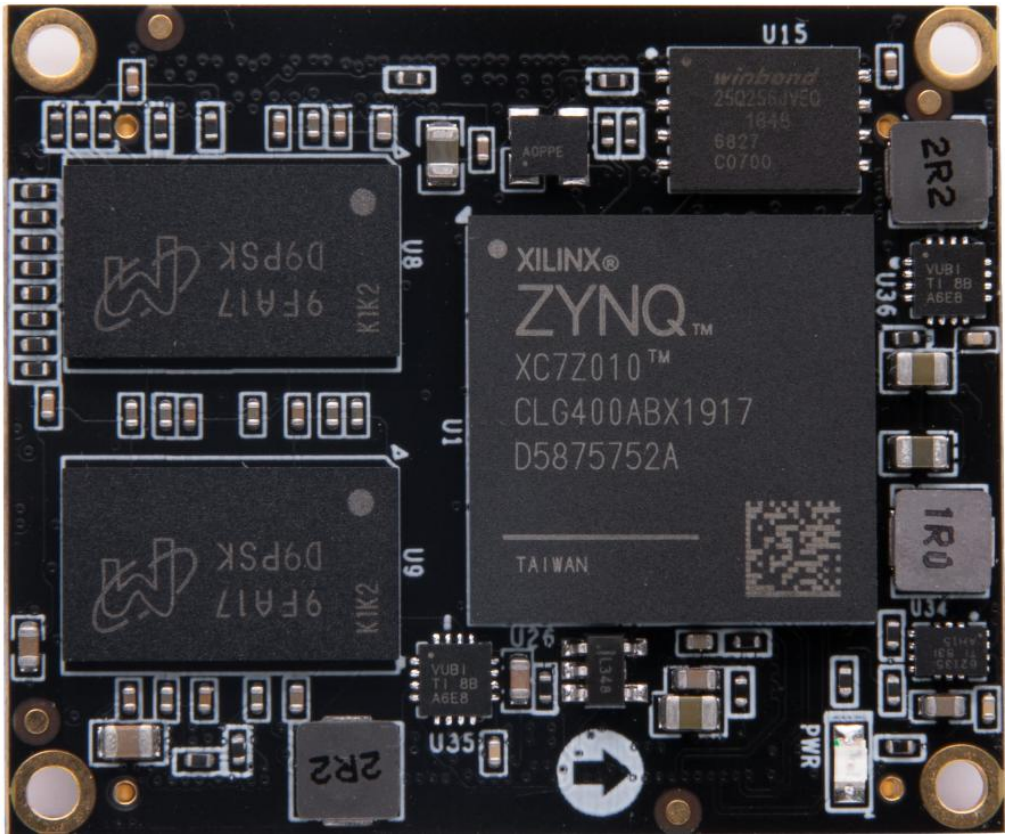


Figure 2-1-1: AC7Z010 Core Board (Front View)

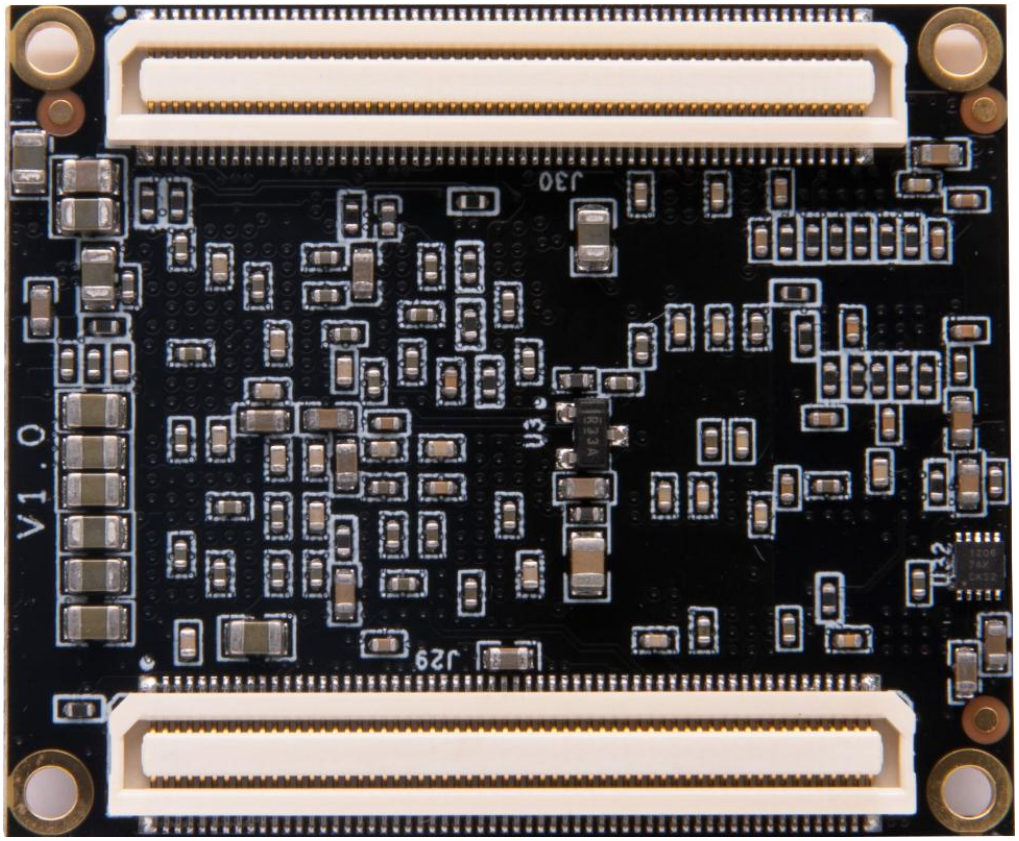


Figure 2-1-2: AC7Z100 Core Board (Rear View)

Part 2.2: ZYNQ Chip

The FPGA core board AC7Z010 uses Xilinx's Zynq7000 series chip, module XC7Z010-1CLG400I. The chip's PS system integrates two ARM Cortex™-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO etc. The PS can operate independently and start up at power on or reset. Figure 2-2-1 detailed the Overall Block Diagram of the ZYNQ7000 Chip.

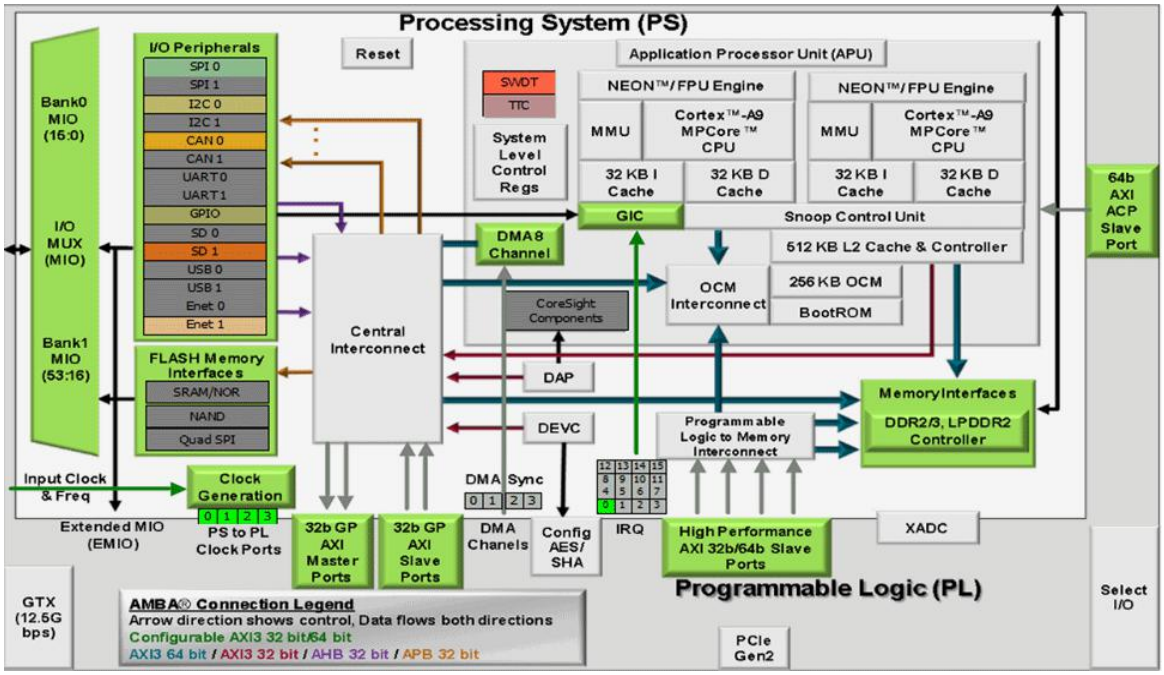


Figure 2-2-1: Overall Block Diagram of the ZYNQ7000 Chip

The main parameters of the PS system part are as follows:

- ARM dual-core CortexA9-based application processor, ARM-v7 architecture, up to 800MHz
- 32KB level 1 instruction and data cache per CPU, 512KB level 2 cache 2 CPU shares

- On-chip boot ROM and 256KB on-chip RAM
- External storage interface, support 16/32 bit DDR2, DDR3 interface
- Two Gigabit NIC support: divergent-aggregate DMA, GMII, RGMII, SGMII interface
- Two USB2.0 OTG interfaces, each supporting up to 12 nodes
- Two CAN2.0B bus interfaces
- Two SD card, SDIO, MMC compatible controllers
- 2 SPIs, 2 UARTs, 2 I2C interfaces
- 4 pairs of 32bit GPIO, 54 (32 + 22) as PS system IO, 64 connected to PL
- High bandwidth connection within PS and PS to PL

The main parameters of the PL logic part are as follows:

- Logic Cells: 28K
- Look-up-tables (LUTs): 17600
- Flip-flops: 35,200
- 18x25MACCs: 80
- Block RAM: 240KB
- Two AD converters for on-chip voltage, temperature sensing and up to 17 external differential input channels, 1MBPS

XC7Z100-1CLG400I chip speed grade is -1, industrial grade, package is BGA400, pin pitch is 0.8mm the specific chip model definition of ZYNQ7000 series is shown in Figure 2-2-2

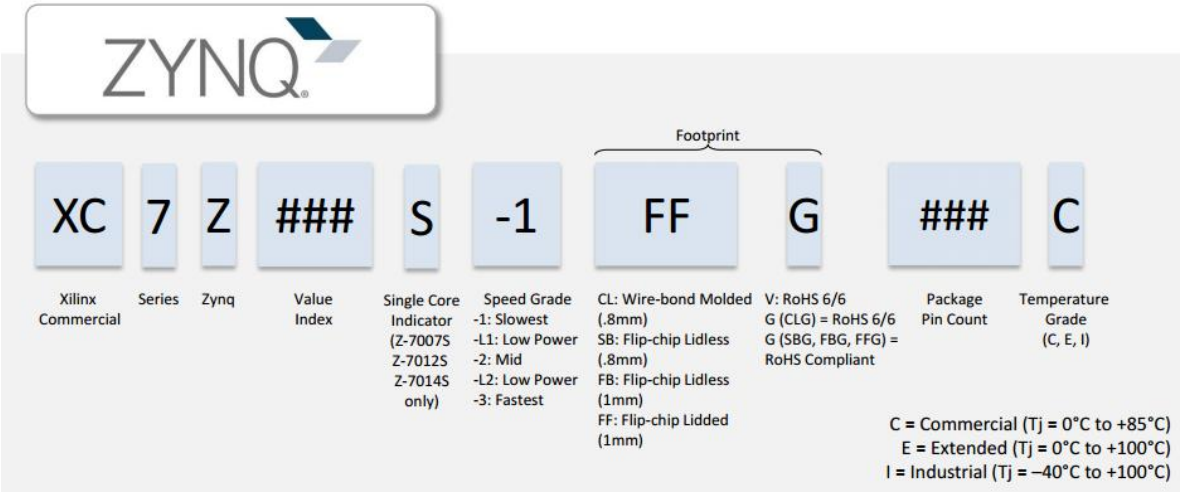


Figure 2-2-2: The Specific Chip Model Definition of ZYNQ7000 Series

Figure 2-2-3: The XC7Z010 chip used on the Core Board

Part 2.3: DDR3 DRAM

The FPGA core board AC7Z010 is equipped with two Micron DDR3 SDRAM chips (1GB in total), model MT41K128M16TW-107 (Compatible with Hynix H5TQ2G63AFR-PBI). The total bus width of DDR3 SDRAM is 32bit. DDR3 SDRAM operates at a maximum speed of 533MHz (data rate

1066Mbps). The DDR3 memory system is directly connected to the memory interface of the BANK 502 of the ZYNQ Processing System (PS). The specific configuration of DDR3 SDRAM is shown in Table 2-3-1 below:

Bit Number	Chip Model	Capacity	Factory
U8,U9	MT41K128M16TW-107	256M x 16bit	Micron

Table 2-3-1: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

The hardware connection of DDR3 DRAM is shown in Figure 2-3-1:

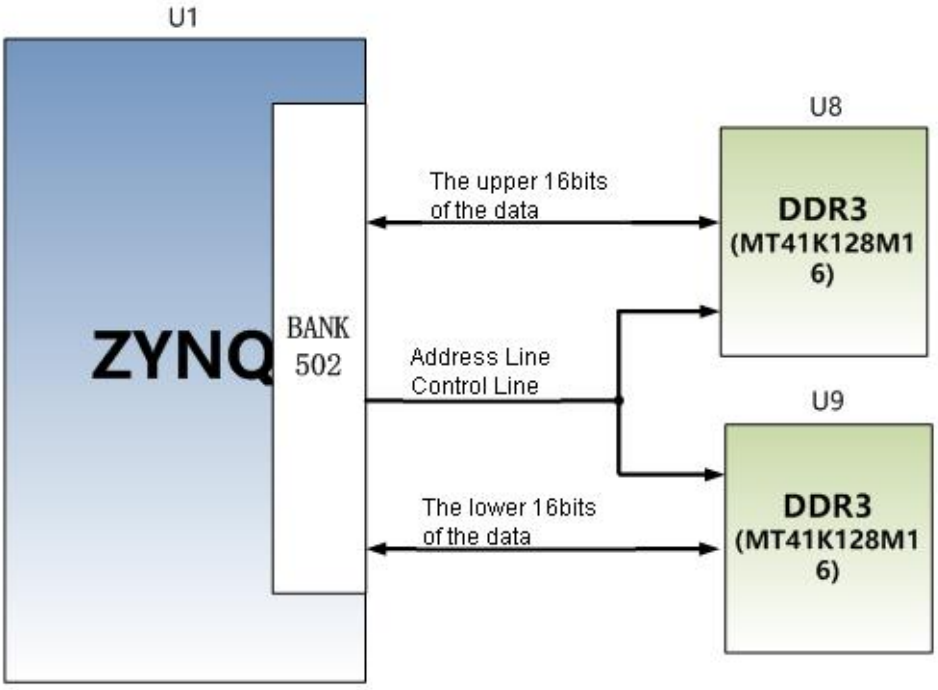


Figure 2-3-1: DDR3 DRAM schematic diagram

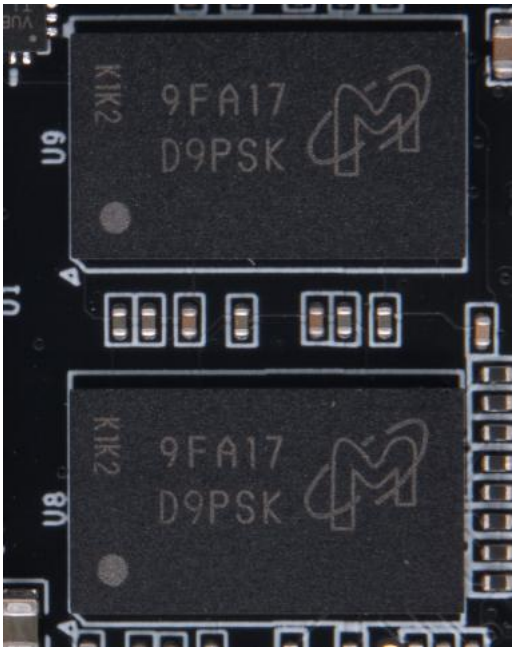


Figure 2-3-2 is the DDR3 DRAM on the core board

DDR3 DRAM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
DDR3_DQS0_P	PS_DDR_DQS_P0_502	C2
DDR3_DQS0_N	PS_DDR_DQS_N0_502	B2
DDR3_DQS1_P	PS_DDR_DQS_P1_502	G2
DDR3_DQS1_N	PS_DDR_DQS_N1_502	F2
DDR3_DQS2_P	PS_DDR_DQS_P2_502	R2
DDR3_DQS2_N	PS_DDR_DQS_N2_502	T2
DDR3_DQS3_P	PS_DDR_DQS_P3_502	W5
DDR3_DQS4_N	PS_DDR_DQS_N3_502	W4
DDR3_D0	PS_DDR_DQ0_502	C3
DDR3_D1	PS_DDR_DQ1_502	B3
DDR3_D2	PS_DDR_DQ2_502	A2
DDR3_D3	PS_DDR_DQ3_502	A4
DDR3_D4	PS_DDR_DQ4_502	D3
DDR3_D5	PS_DDR_DQ5_502	D1
DDR3_D6	PS_DDR_DQ6_502	C1
DDR3_D7	PS_DDR_DQ7_502	E1
DDR3_D8	PS_DDR_DQ8_502	E2
DDR3_D9	PS_DDR_DQ9_502	E3

DDR3_D10	PS_DDR_DQ10_502	G3
DDR3_D11	PS_DDR_DQ11_502	H3
DDR3_D12	PS_DDR_DQ12_502	J3
DDR3_D13	PS_DDR_DQ13_502	H2
DDR3_D14	PS_DDR_DQ14_502	H1
DDR3_D15	PS_DDR_DQ15_502	J1
DDR3_D16	PS_DDR_DQ16_502	P1
DDR3_D17	PS_DDR_DQ17_502	P3
DDR3_D18	PS_DDR_DQ18_502	R3
DDR3_D19	PS_DDR_DQ19_502	R1
DDR3_D20	PS_DDR_DQ20_502	T4
DDR3_D21	PS_DDR_DQ21_502	U4
DDR3_D22	PS_DDR_DQ22_502	U2
DDR3_D23	PS_DDR_DQ23_502	U3
DDR3_D24	PS_DDR_DQ24_502	V1
DDR3_D25	PS_DDR_DQ25_502	Y3
DDR3_D26	PS_DDR_DQ26_502	W1
DDR3_D27	PS_DDR_DQ27_502	Y4
DDR3_D28	PS_DDR_DQ28_502	Y2
DDR3_D29	PS_DDR_DQ29_502	W3
DDR3_D30	PS_DDR_DQ30_502	V2
DDR3_D31	PS_DDR_DQ31_502	V3
DDR3_DM0	PS_DDR_DM0_502	A1
DDR3_DM1	PS_DDR_DM1_502	F1
DDR3_DM2	PS_DDR_DM2_502	T1
DDR3_DM3	PS_DDR_DM3_502	Y1
DDR3_A0	PS_DDR_A0_502	N2
DDR3_A1	PS_DDR_A1_502	K2
DDR3_A2	PS_DDR_A2_502	M3
DDR3_A3	PS_DDR_A3_502	K3
DDR3_A4	PS_DDR_A4_502	M4
DDR3_A5	PS_DDR_A5_502	L1
DDR3_A6	PS_DDR_A6_502	L4
DDR3_A7	PS_DDR_A7_502	K4
DDR3_A8	PS_DDR_A8_502	K1
DDR3_A9	PS_DDR_A9_502	J4

DDR3_A10	PS_DDR_A10_502	F5
DDR3_A11	PS_DDR_A11_502	G4
DDR3_A12	PS_DDR_A12_502	E4
DDR3_A13	PS_DDR_A13_502	D4
DDR3_A14	PS_DDR_A14_502	F4
DDR3_BA0	PS_DDR_BA0_502	L5
DDR3_BA1	PS_DDR_BA1_502	R4
DDR3_BA2	PS_DDR_BA2_502	J5
DDR3_S0	PS_DDR_CS_B_502	N1
DDR3_RAS	PS_DDR_RAS_B_502	P4
DDR3_CAS	PS_DDR_CAS_B_502	P5
DDR3_WE	PS_DDR_WE_B_502	M5
DDR3_ODT	PS_DDR_ODT_502	N5
DDR3_RESET	PS_DDR_DRST_B_502	B4
DDR3_CLK0_P	PS_DDR_CKP_502	L2
DDR3_CLK0_N	PS_DDR_CKN_502	M2
DDR3_CKE	PS_DDR_CKE_502	N3

Part 2.4: QSPI Flash

The FPGA core board AC7Z010 is equipped with one 256MBit Quad-SPI FLASH chip, the flash model is W25Q256FVEI, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 2-4-1.

Position	Model	Capacity	Factory
U15	W25Q256FVEI	32M Byte	Winbond

Table 2-4-1: QSPI FLASH Specification

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of

these PS ports need to be configured as the QSPI FLASH interface. Figure 2-4-1 shows the QSPI Flash in the schematic.

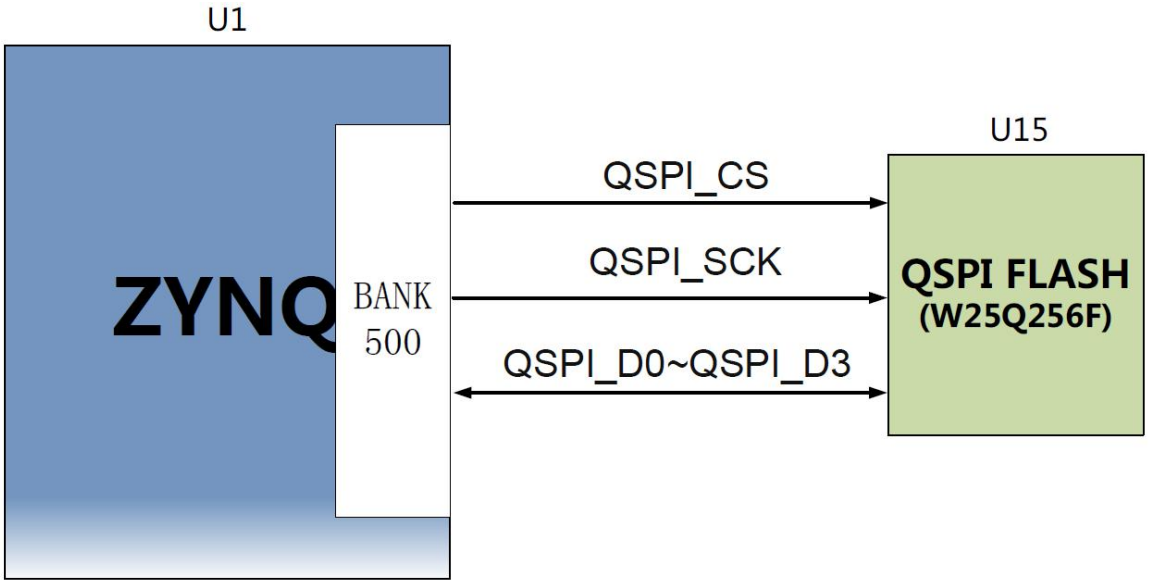


Figure 2-4-1: QSPI Flash in the schematic

Figure 2-4-2 is the QSPI Flash on the core board

Configure chip pin assignments:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
QSPI_SCK	PS_MIO6_500	A5
QSPI_CS	PS_MIO1_500	A7
QSPI_D0	PS_MIO2_500	B8
QSPI_D1	PS_MIO3_500	D6
QSPI_D2	PS_MIO4_500	B7
QSPI_D3	PS_MIO5_500	A6

Part 2.5: Clock configuration

The AC7Z010 core board provides an active clock for the PS system, so that the PS system can work independently.

PS system clock source

The ZYNQ chip provides 33.333333MHz clock input for the PS part through the X1 crystal on the core board. The clock input is connected to the PS_CLK_500 pin of the ZYNQ chip BANK500. Its schematic diagram is shown in Figure 2-5-1:

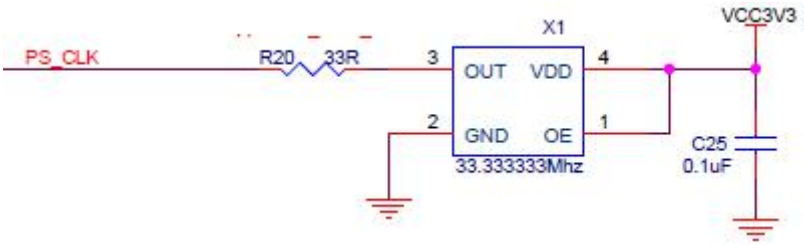


Figure 2-5-1: Active crystal of PS part

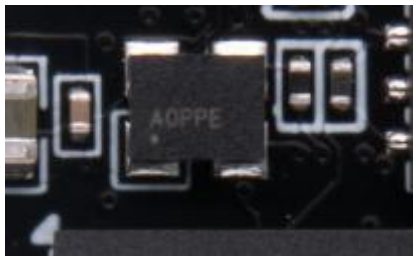


Figure 2-5-2: 33.333333Mhz active crystal on the core board

Clock pin assignment:

Signal name	ZYNQ Pin
PS_CLK_500	E7

Part 2.6: Power Supply

The power supply voltage of the AC7Z010 core board is DC5V, which is supplied by connecting the carrier board. In addition, the power of BANK34 and

BANK35 is also provided through the carrier board. The schematic diagram of the power supply design on the core board is shown in Figure 2-6-1:

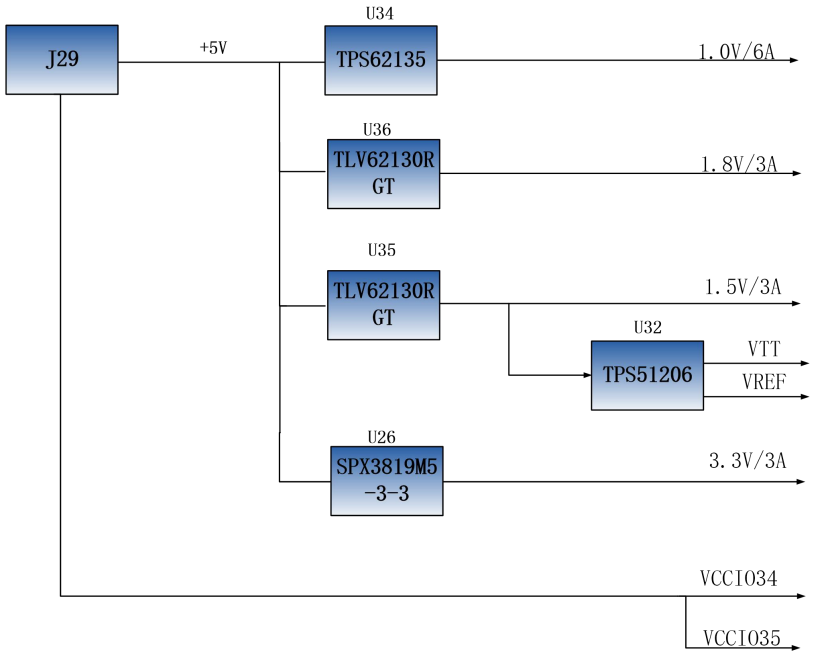


Figure 2-6-1 Power interface part in the schematic diagram

The FPGA development board is powered by + 5V, and is converted into + 1.0V, + 1.8V, + 1.5V, + 3.3V four power supplies through four DC / DC power chips. The output current of + 1.0V can reach 6A, + 1.8V and + 1.5V power output current is 3A, + 3.3V output current is 500mA. J29 also has 4 pins each to supply power to FPGA BANK34 and BANK35. The default is 3.3V. Users can change the power of BANK34 and BANK35 by changing VCCIO34 and VCCIO35 on the backplane. 1.5V generates the VTT and VREF voltages required by DDR3 through TI's TPS51206. The functions of each power distribution are shown in the following table:

Power Supply	Function
+1.0V	ZYNQ PS and PL section Core Voltage
+1.8V	ZYNQ PS and PL partial auxiliary voltage BANK501 IO voltage
+3.3V	ZYNQ Bank0,Bank500,QSIP FLASH Clock Crystal

+1.5V	DDR3, ZYNQ Bank501
VREF,VTT(+0.75V)	DDR3
VCCIO34/35	Bank34, Bank35

Because the power supply of the ZYNQ FPGA has the power-on sequence requirements, in the circuit design, we have designed according to the power requirements of the chip. The power-on sequence is +1.0V->+1.8V->(+1.5 V, +3.3V, VCCIO) circuit design to ensure the normal operation of the chip. Because the level standards of BANK34 and BANK35 are determined by the power supply provided by the carrier board, the highest is 3.3V. When you design the carrier board to provide the VCCIO34 and VCCIO35 power for the core board, the power-on sequence is slower than + 5V.

Part 2.7: AC7Z010 Core Board Size Dimension

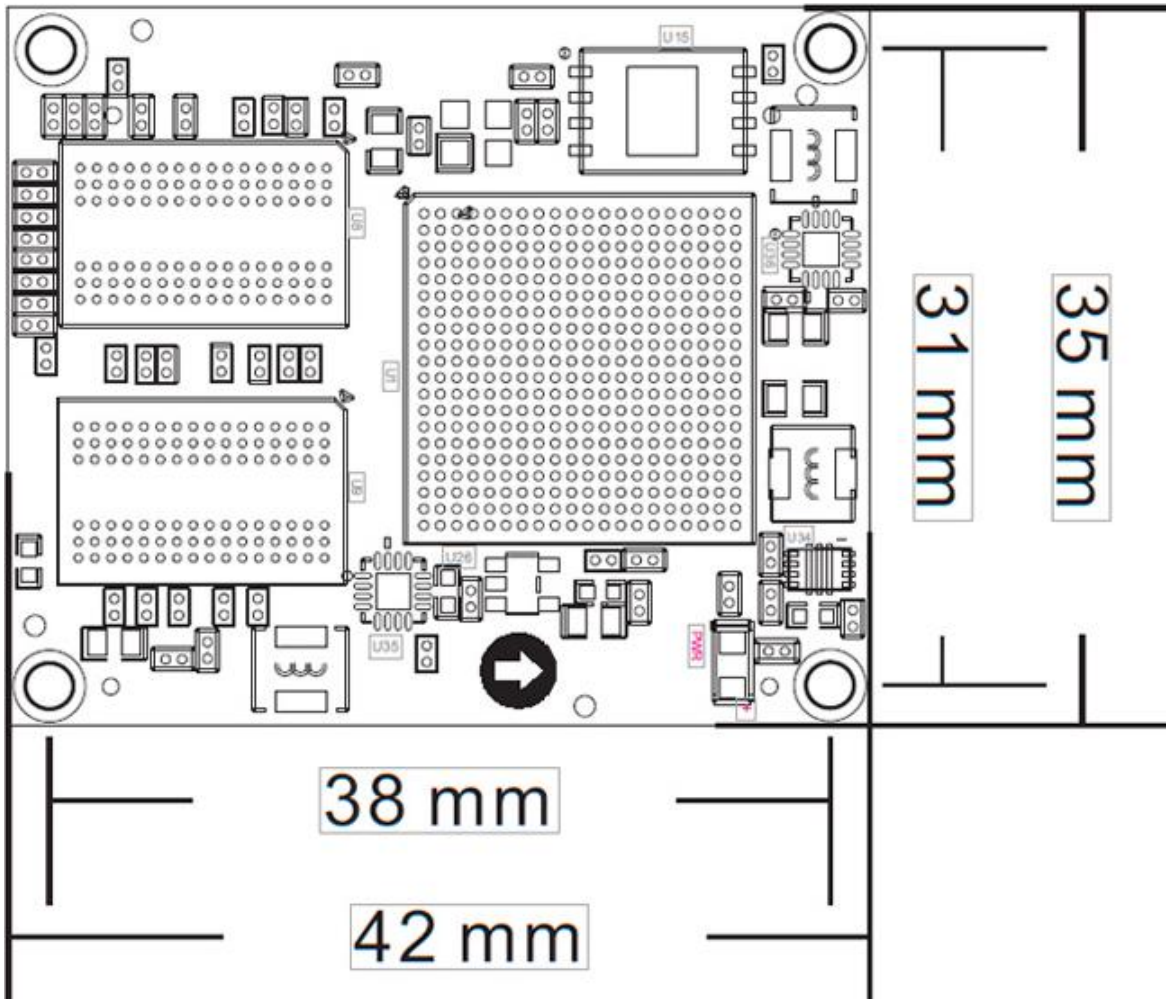


Figure 2-7-1: AC7Z010 Core Board Size Dimension

Part 2.8: Board to Board Connectors pin assignment

The core board has a total of two high-speed expansion ports. It uses two 120-pin inter-board connectors (J29/J30) to connect to the carrier board. The PIN spacing of the board to board connector is 0.5mm, among them, J29 is connected to 5V power, VCCIO power input, some IO signals and JTAG signals, and J30 is connected to the remaining IO signals and MIO. The IO level of BANK34 and BANK35 can be changed by adjusting the VCCIO input on the connector, the highest level does not exceed 3.3V. The AX7Z010 carrier board we designed is 3.3V by default. **Note that the IO of BANK13 is not**

available for AC7Z010 core board.

Pin assignment of board to board connector J29

J29 Pin	Signal Name	ZYNQ Pin Number	J29 Pin	Signal Name	ZYNQ Pin Number
1	VCC5V	-	2	VCC5V	-
3	VCC5V	-	4	VCC5V	-
5	VCC5V	-	6	VCC5V	-
7	VCC5V	-	8	VCC5V	-
9	GND	-	10	GND	-
11	VCCIO_34	-	12	VCCIO_35	-
13	VCCIO_34	-	14	VCCIO_35	-
15	VCCIO_34	-	16	VCCIO_35	-
17	VCCIO_34	-	18	VCCIO_35	-
19	GND	-	20	GND	-
21	IO34_L10P	V15	22	IO34_L7P	Y16
23	IO34_L10N	W15	24	IO34_L7N	Y17
25	IO34_L15N	U20	26	IO34_L17P	Y18
27	IO34_L15P	T20	28	IO34_L17N	Y19
29	GND	-	30	GND	-
31	IO34_L9N	U17	32	IO34_L8P	W14
33	IO34_L9P	T16	34	IO34_L8N	Y14
35	IO34_L12N	U19	36	IO34_L3P	U13
37	IO34_L12P	U18	38	IO34_L3N	V13
39	GND	-	40	GND	-
41	IO34_L14N	P20	42	IO34_L21N	V18
43	IO34_L14P	N20	44	IO34_L21P	V17
45	IO34_L16N	W20	46	IO34_L18P	V16
47	IO34_L16P	V20	48	IO34_L18N	W16
49	GND	-	50	GND	-
51	IO34_L22N	W19	52	IO34_L23P	N17
53	IO34_L22P	W18	54	IO34_L23N	P18
55	IO34_L20N	R18	56	IO34_L13N	P19
57	IO34_L20P	T17	58	IO34_L13P	N18
59	GND	-	60	GND	-

61	IO34_L19N	R17	62	IO34_L11N	U15
63	IO34_L19P	R16	64	IO34_L11P	U14
65	IO34_L24P	P15	66	IO34_L5N	T15
67	IO34_L24N	P16	68	IO34_L5P	T14
69	GND	-	70	GND	-
71	IO34_L4P	V12	72	IO34_L2N	U12
73	IO34_L4N	W13	74	IO34_L2P	T12
75	IO34_L1P	T11	76	IO34_L6N	R14
77	IO34_L1N	T10	78	IO34_L6P	P14
79	GND	-	80	GND	-
81	IO13_L13P	Y7	82	IO13_L21P	V11
83	IO13_L13N	Y6	84	IO13_L21N	V10
85	IO13_L11N	V7	86	IO13_L14N	Y8
87	IO13_L11P	U7	88	IO13_L14P	Y9
89	GND	-	90	GND	-
91	IO13_L19N	U5	92	IO13_L22N	W6
93	IO13_L19P	T5	94	IO13_L22P	V6
95	IO13_L16P	W10	96	IO13_L15P	V8
97	IO13_L16N	W9	98	IO13_L15N	W8
99	GND	-	100	GND	-
101	IO13_L17P	U9	102	IO13_L20P	Y12
103	IO13_L17N	U8	104	IO13_L20N	Y13
105	IO13_L18P	W11	106	IO13_L12N	U10
107	IO13_L18N	Y11	108	IO13_L12P	T9
109	GND	-	110	GND	-
111	FPGA_TCK	F9	112	VP	K9
113	FPGA_TMS	J6	114	VN	L10
115	FPGA_TDO	F6	116	PS_POR_B	C7
117	FPGA_TDI	G6	118	FPGA_DONE	R11

Pin assignment of board to board connector J30

J30 Pin	Signal Name	ZYNQ Pin Number	J30 Pin	Signal Name	ZYNQ Pin Number
1	IO35_L1P	C20	2	IO35_L15N	F20

3	IO35_L1N	B20	4	IO35_L15P	F19
5	IO35_L18N	G20	6	IO35_L5P	E18
7	IO35_L18P	G19	8	IO35_L5N	E19
9	GND	T13	10	GND	T13
11	IO35_L10N	J19	12	IO35_L3N	D18
13	IO35_L10P	K19	14	IO35_L3P	E17
15	IO35_L2N	A20	16	IO35_L4P	D19
17	IO35_L2P	B19	18	IO35_L4N	D20
19	GND	T13	20	GND	T13
21	IO35_L8P	M17	22	IO35_L9N	L20
23	IO35_L8N	M18	24	IO35_L9P	L19
25	IO35_L7P	M19	26	IO35_L6P	F16
27	IO35_L7N	M20	28	IO35_L6N	F17
29	GND	T13	30	GND	T13
31	IO35_L17N	H20	32	IO35_L16N	G18
33	IO35_L17P	J20	34	IO35_L16P	G17
35	IO35_L19N	G15	36	IO35_L13N	H17
37	IO35_L19P	H15	38	IO35_L13P	H16
39	GND	T13	40	GND	T13
41	IO35_L12N	K18	42	IO35_L14N	H18
43	IO35_L12P	K17	44	IO35_L14P	J18
45	IO35_L24N	J16	46	IO35_L20P	K14
47	IO35_L24P	K16	48	IO35_L20N	J14
49	GND	T13	50	GND	T13
51	IO35_L21N	N16	52	IO35_L11P	L16
53	IO35_L21P	N15	54	IO35_L11N	L17
55	IO35_L22N	L15	56	IO35_L23P	M14
57	IO35_L22P	L14	58	IO35_L23N	M15
59	GND	T13	60	GND	T13
61	PS_MIO22	B17	62	PS_MIO50	B13
63	PS_MIO27	D13	64	PS_MIO45	B15
65	PS_MIO23	D11	66	PS_MIO46	D16
67	PS_MIO24	A16	68	PS_MIO41	C17
69	GND	T13	70	GND	T13
71	PS_MIO25	F15	72	PS_MIO7	D8
73	PS_MIO26	A15	74	PS_MIO12	D9

75	PS_MIO21	F14	76	PS_MIO10	E9
77	PS_MIO16	A19	78	PS_MIO11	C6
79	GND	T13	80	GND	T13
81	PS_MIO20	A17	82	PS_MIO9	B5
83	PS_MIO19	D10	84	PS_MIO14	C5
85	PS_MIO18	B18	86	PS_MIO8	D5
87	PS_MIO17	E14	88	PS_MIO0	E6
89	GND	T13	90	GND	T13
91	PS_MIO39	C18	92	PS_MIO13	E8
93	PS_MIO38	E13	94	PS_MIO47	B14
95	PS_MIO37	A10	96	PS_MIO48	B12
97	PS_MIO28	C16	98	PS_MIO49	C12
99	GND	T13	100	GND	T13
101	PS_MIO35	F12	102	PS_MIO52	C10
103	PS_MIO34	A12	104	PS_MIO51	B9
105	PS_MIO33	D15	106	PS_MIO40	D14
107	PS_MIO32	A14	108	PS_MIO44	F13
109	GND	T13	110	GND	T13
111	PS_MIO31	E16	112	PS_MIO15	C8
113	PS_MIO36	A11	114	PS_MIO42	E12
115	PS_MIO29	C13	116	PS_MIO43	A9
117	PS_MIO30	C15	118	PS_MIO53	C11
119	QSPI_D3_PS_MIO5	A6	120	QSPI_D2_PS_MIO4	B7

Part 3: Carrier Board

Part 3.1: Carrier Board Introduction

Through the previous function introduction, you can understand the function of the carrier board part

- 2-Channel CAN communication interfaces
- 2-Channel 485 communication interfaces
- 1-Channel 10/100M/1000M Ethernet RJ-45 interface
- 1-Channel USB HOST interface
- 1-Channel USB Uart communication interface
- 1-Channel SD card slot
- 2-Channel 40-pin expansion port
- 2-Channel AD input interfaces
- 1-Channel HDMI video output interface
- 1-Channel MIPI camera interface (only for AX7Z020)
- 1-Channel RTC real-time clock
- 1-Channel EEPROM
- 1-Channel temperature sensor
- JTAG debugging interface
- 4 independent keys
- 4 user LED lights

Part 3.2: CAN communication interface

There are 2 CAN communication interfaces on the AX7Z010 carrier board, which are connected to the GPIO interface of the BANK500 on the PS system side. The CAN transceiver chip selected TI's SN65HVD232C chip for user CAN communication services.

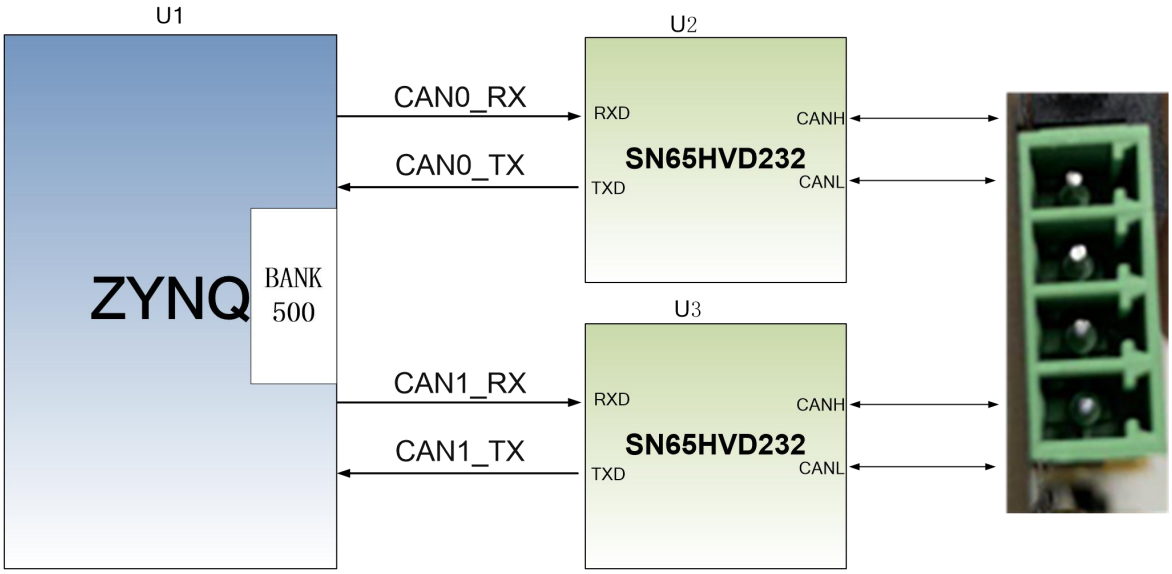


Figure 3-2-1: Connection diagram of CAN transceiver chip on PS side

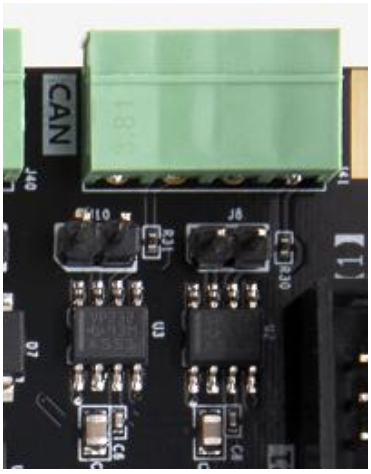


Figure 3-2-2: CAN chip and interface of PS side on the carrier board

The CAN communication pin assignments are as follows:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
CAN0_RX	PS_MIO10	E9	CAN0 Receiver
CAN0_TX	PS_MIO11	C6	CAN0 Transmitter
CAN1_RX	PS_MIO13	E8	CAN1 Receiver
CAN1_TX	PS_MIO12	D9	CAN1 Transmitter

Part 3.3: 485 communication interface

There are two 485 communication interfaces on the AX7Z010 carrier board. Among them, 485 communication port 1 is connected to the GPIO interface of BANK500 on the PS system, and 485 communication port 2 is connected to the GPIO interface of BANK34 on the PL system.

The 485 transceiver chip selects the MAX3485 chip from MAXIM for the user's 485 communication service.

Figure 3-3-1 is the connection diagram of the 485 transceiver chip on the PL side

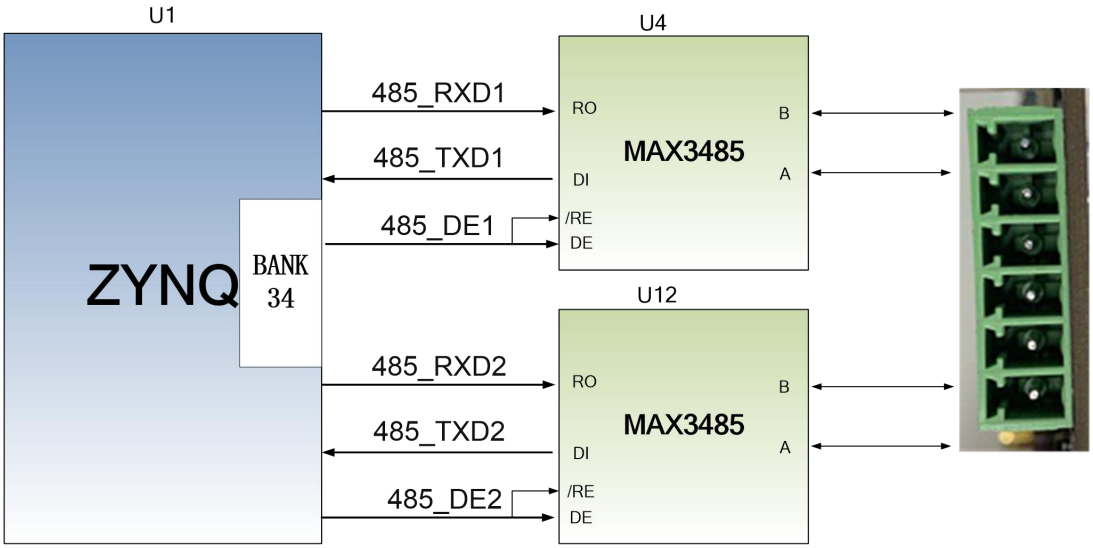


Figure 3-3-1: RS485 chip and interface connection diagram

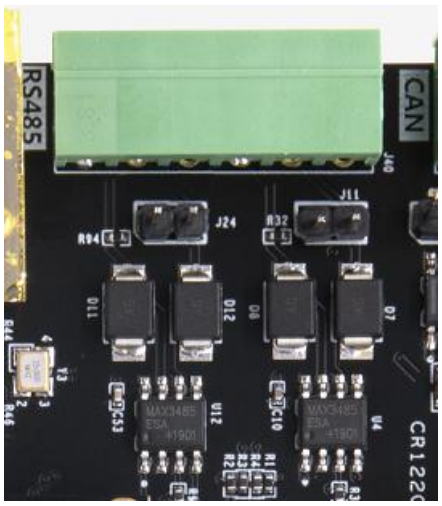


Figure 3-3-2: RS485 chip and interface on the carrier board

The 485 communication pins are assigned as follows:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
485_TXD1	PS_MIO15	C8	485 Transmitter 1
485_RXD1	PS_MIO14	C5	485 Receiver 1
485_DE1	PS_MIO9	B5	485 Receive launch enable 1
485_TXD2	IO34_L4N	W13	485 Transmitter 2
485_RXD2	IO34_L4P	V12	485 Receiver 2
485_DE2	IO34_L12N	U19	485 Receive launch enable 2

Part 3.4: Gigabit Ethernet Interface

The AX7Z010 carrier board has 1 Gigabit Ethernet interface, which is connected to the GPIO interface of BANK501 on the PS system side. The Ethernet chip uses Micrel's KSZ9031RNX Ethernet PHY chip to provide users with network communication services. The KSZ9031RNX chip supports 10/100/1000 Mbps network transmission rate, and performs data communication with the MAC layer of the Zynq7000 system through the RGMII interface. KSZ9031RNX supports MDI / MDX adaptive, various speeds adaptive, Master / Slave adaptive, supports MDIO bus for PHY register management.

When the KSZ9031RNX is powered on, it will detect the level status of some specific IOs to determine its own operating mode. Table 3-4-1 describes the default settings after the GPHY chip is powered on.

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address 011
CLK125_EN	Enable 125Mhz clock output selection	Enable
LED_MODE	LED light mode configuration	Single LED light mode
MODE0~MODE3	Link adaptation and full duplex configuration	10/100/1000 adaptive, compatible with full-duplex, half-duplex

Table 3-4-1: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of ZYNQ and PHY chip KSZ9031RNX is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising edge and falling samples of the clock.

When the network is connected to 100M Ethernet, the data transmission of ZYNQ and PHY chip KSZ9031RNX is communicated through RMII bus, and the transmission clock is 25Mhz. Data is sampled on the rising edge and falling samples of the clock.

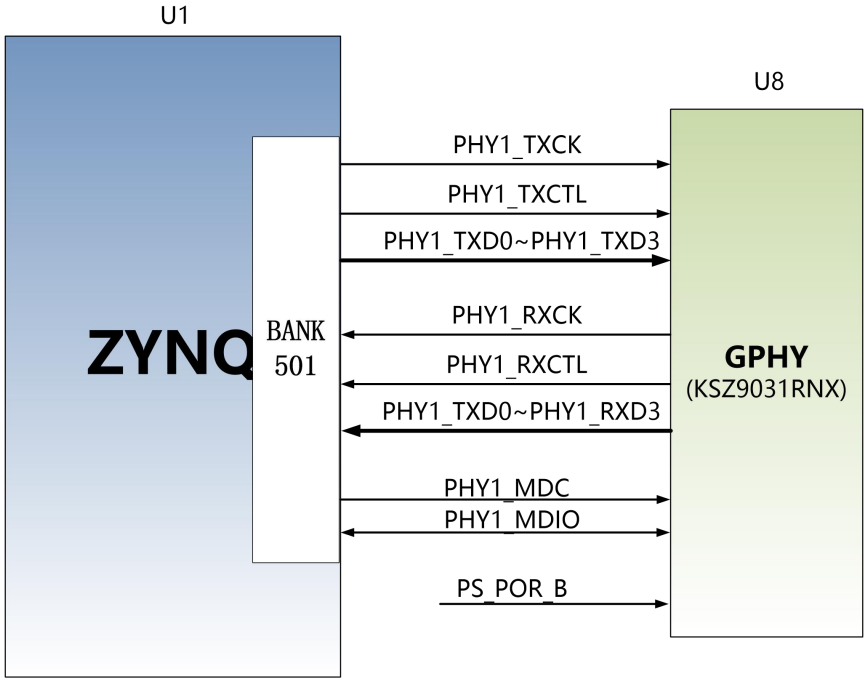


Figure 3-4-1: ZYNQ PS system and GPHY connection diagram

Figure 3-4-2: Ethernet GPHY chip and interface on the carrier board

The Gigabit Ethernet pin assignments are as follows:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
ETH_TXCK	PS_MIO16	A19	RGMII Transmit Clock
ETH_TXD0	PS_MIO17	E14	Transmit data bit0
ETH_TXD1	PS_MIO18	B18	Transmit data bit1
ETH_TXD2	PS_MIO19	D10	Transmit data bit2
ETH_TXD3	PS_MIO20	A17	Transmit data bit3
ETH_TXCTL	PS_MIO21	F14	Transmit enable signal
ETH_RXCK	PS_MIO22	B17	RGMII Receive Clock
ETH_RXD0	PS_MIO23	D11	Receive data Bit0
ETH_RXD1	PS_MIO24	A16	Receive data Bit1
ETH_RXD2	PS_MIO25	F15	Receive data Bit2
ETH_RXD3	PS_MIO26	A15	Receive data Bit3
ETH_RXCTL	PS_MIO27	D13	Receive data valid signal
ETH_MDC	PS_MIO52	C10	MDIO Management clock
ETH_MDIO	PS_MIO53	C11	MDIO Management data
PS_POR_B	PS_POR_B	C7	Reset signal

Part 3.5: USB2.0 Host Interface

There is 1 USB2.0 HOST interfaces on the AX7Z010 FPGA carrier board. The USB2.0 transceiver uses a 1.8V, high-speed USB3320C-EZK chip that supports the ULPI standard interface. ZYNQ's USB bus interface is connected to the USB3320C-EZK transceiver to achieve high-speed USB2.0 Host mode data communication. USB3320C's USB data and control signals are connected to the IO port of BANK501 on the PS side of the ZYNQ chip. The 24MHz crystal provides the system clock for the USB3320C chip.

The USB port is flat USB ports (USB Type A), which allows users to connect different USB Slave peripherals (such as USB mouse and USB keyboard) at the same time. In addition, the carrier board provides + 5V power for the USB port.

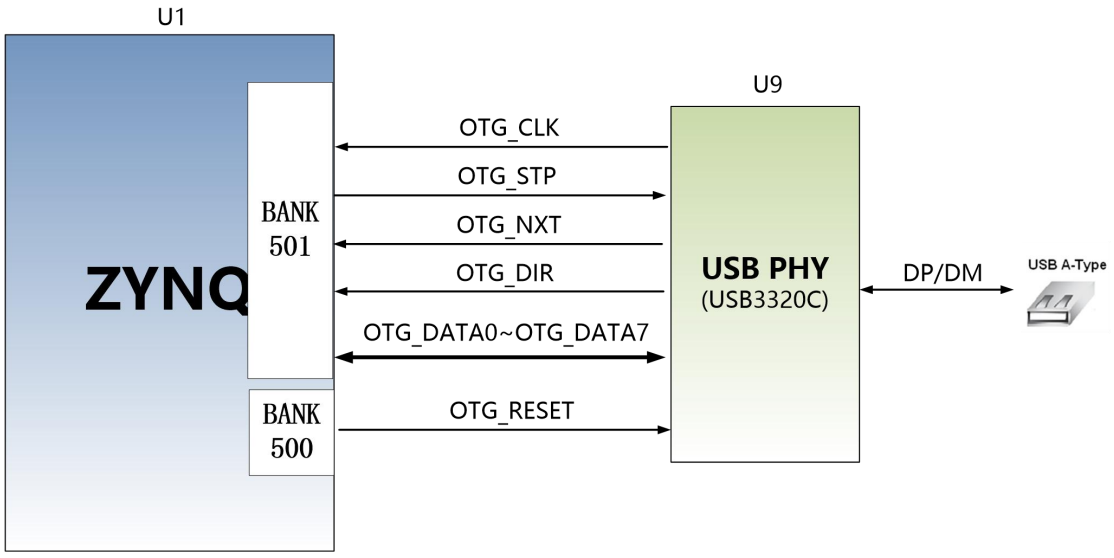


Figure 3-5-1: The connection between Zynq7000 and USB chip

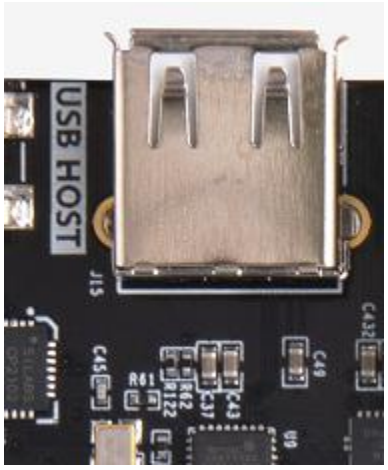


Figure 3-5-2: USB2.0 on the carrier board

USB2.0 Pin Assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
OTG_DATA4	PS_MIO28	C16	USB Data Bit4
OTG_DIR	PS_MIO29	C13	USB Data Direction Signal
OTG_STP	PS_MIO30	C15	USB Stop Signal
OTG_NXT	PS_MIO31	E16	USB Next Data Signal
OTG_DATA0	PS_MIO32	A14	USB Data Bit0
OTG_DATA1	PS_MIO33	D15	USB Data Bit1
OTG_DATA2	PS_MIO34	A12	USB Data Bit2
OTG_DATA3	PS_MIO35	F12	USB Data Bit3
OTG_CLK	PS_MIO36	A11	USB Clock Signal

OTG_DATA5	PS_MIO37	A10	USB Data Bit5
OTG_DATA6	PS_MIO38	E13	USB Data Bit6
OTG_DATA7	PS_MIO39	C18	USB Data Bit7
OTG_RESETN	PS_MIO46	D16	USB Reset Signal

Part 3.6: USB to Serial Port

The AX7Z010 FPGA carrier board is equipped with a Uart to USB interface for overall debugging of ZYNQ7000 system. The conversion chip uses the USB-UAR chip of Silicon Labs CP2102GM. The USB interface uses the MINI USB interface. It can be connected to the USB port of the upper PC with a USB cable for separate power supply and serial data communication of the core board.

The schematic diagram of the USB Uart circuit design is shown in Figure 3-6-1:

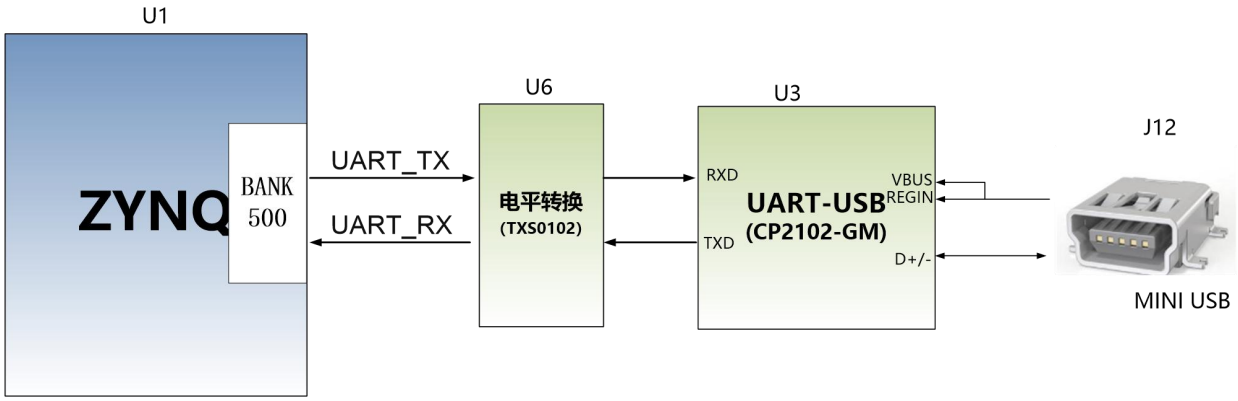


Figure 3-6-1: USB to serial port schematic

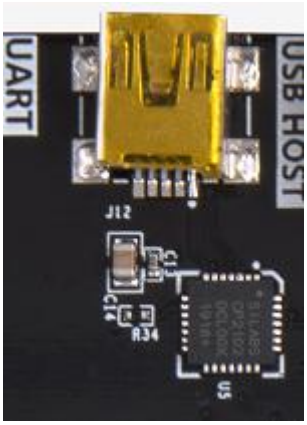


Figure 3-6-2: USB to serial port on the AX7Z010 Carrier Board

USB to serial port ZYNQ pin assignment:

Signal name	ZYNQ Pin Name	ZYNQ Pin Number	Description
UART_RX	PS_MIO49	C12	Uart data input
UART_TX	PS_MIO48	B12	Uart data output

Part 3.7: AD input interface

The AX7Z010 carrier board is equipped with four AD input interfaces, two of which are used to collect external analog signals for AD conversion, and the other two are used to measure the power supply voltage and current of the FPGA development board. The two analog signals used to collect external analog signals for AD conversion use SMA connectors as inputs, convert the input signals into differential signals, and then enter ZYNQ. Supply current measurement is connected to the dedicated AD input pins VP and VN of ZYNQ.

The schematic diagram of the AD acquisition circuit design is shown in Figure 3-7-1 below:

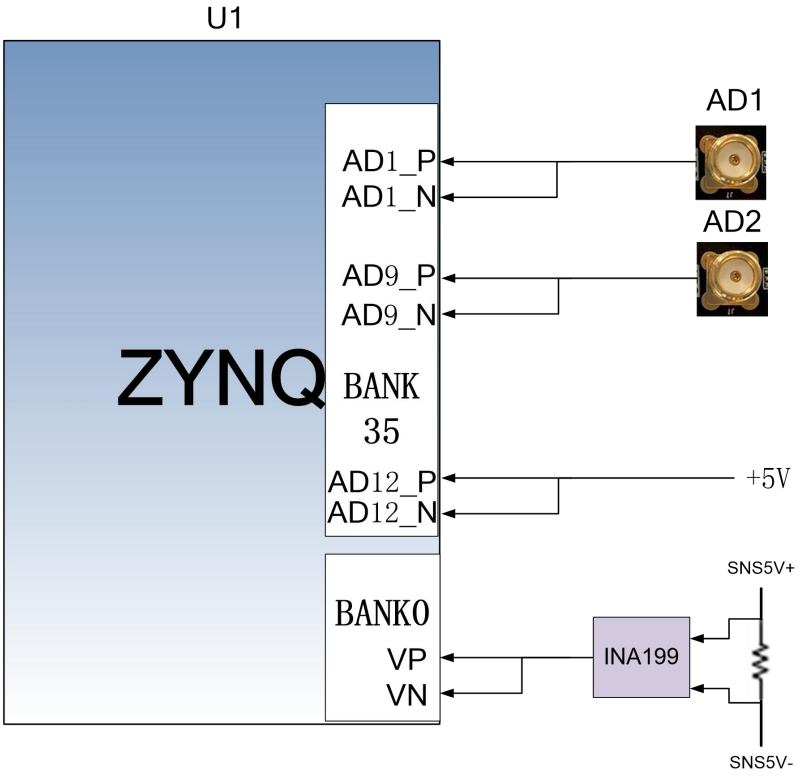


Figure 3-7-1: AD acquisition circuit Schematic

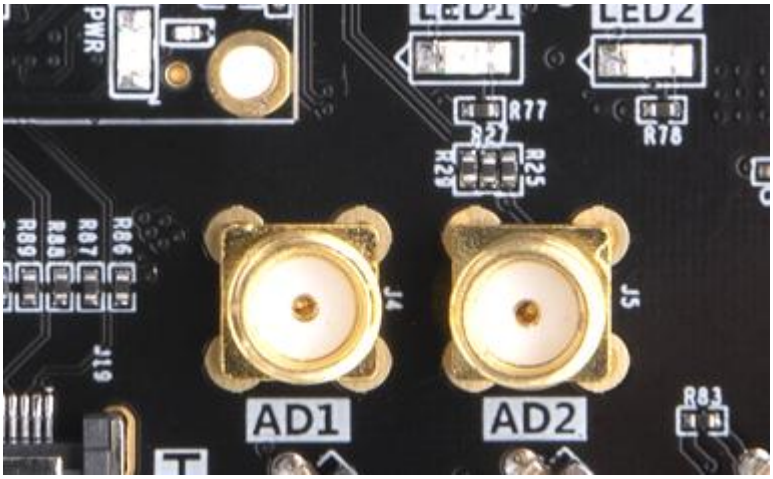


Figure 3-7-2: AD acquisition circuit interface on the carrier board

ZYNQ pin assignment of AD acquisition circuit:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
XADC_AD1P	IO35_L3P	E17	AD_IN_P
XADC_AD1N	IO35_L3N	D18	AD_IN_N
XADC_AD9P	IO35_L5P	E18	AD_IN_P
XADC_AD9N	IO35_L5N	E19	AD_IN_N
XADC_AD12P	IO35_L15P	F19	AD_IN_P
XADC_AD12N	IO35_L15N	F20	AD_IN_N
VP	VP	K9	AD_IN_P
VN	VN	L10	AD_IN_N

Part 3.8: HDMI Output Interface

HDMI, full name is high-definition multimedia video output interface. The AX7Z010 development board is directly connected to the differential signal and clock of the HDMI interface through the differential IO of ZYNQ, and the differential conversion of HMDI signals in ZYNQ is performed in parallel and then coded to realize the transmission solution of DMI digital video input and output. The highest support 1080P @ 60Hz input and output function.

The HDMI signal is connected to BANK34 in the PL part of ZYNQ. The schematic diagram of the design is shown in Figure 3-8-1 below:

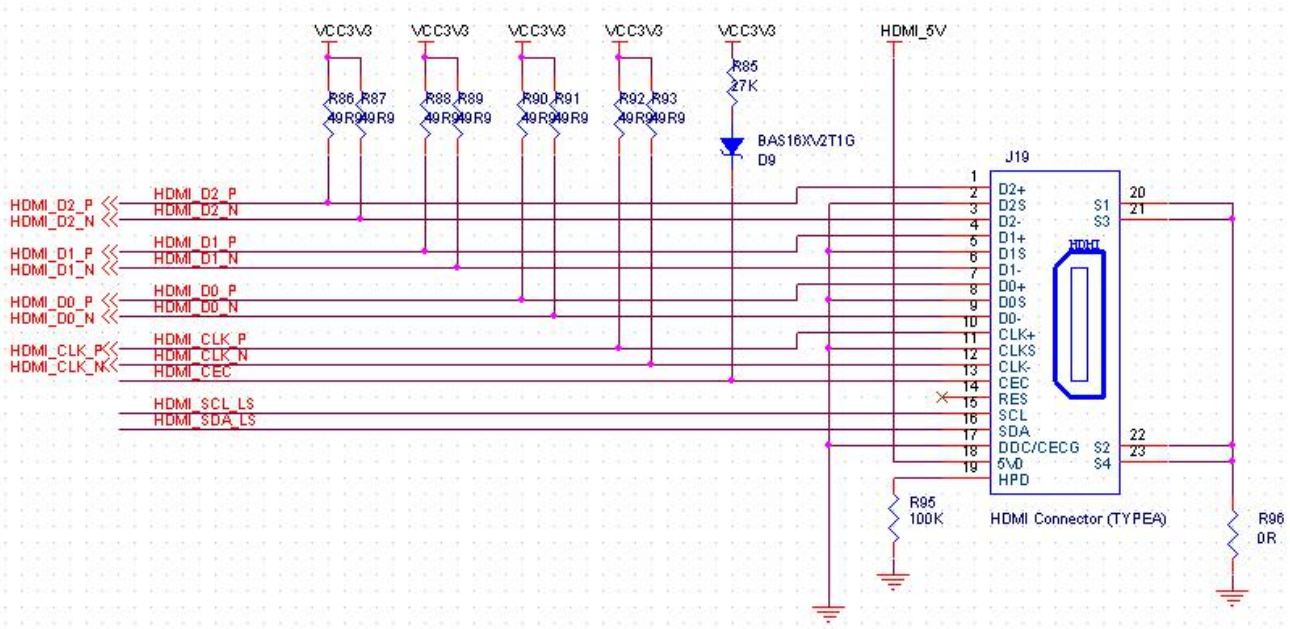


Figure 3-8-1: HDMI Output Interface Design Schematic

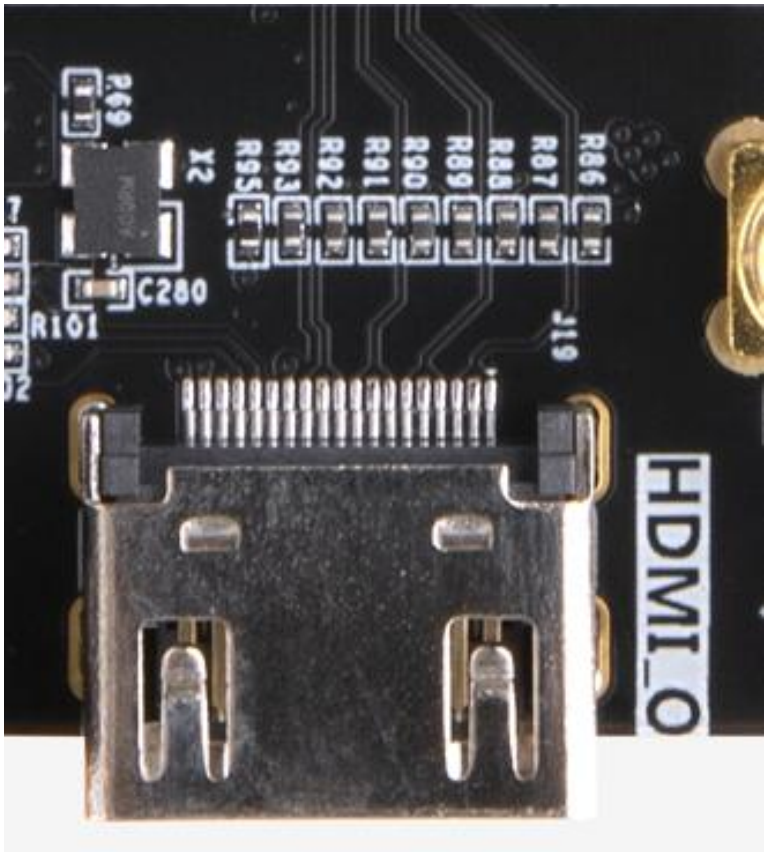


Figure 3-8-2: HDMI Output Interface on the carrier board

ZYNQ Pin Assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
HDMI_CLK_P	IO34_L3P	U13	HDMI clock signal Positive
HDMI_CLK_N	IO34_L3N	V13	HDMI clock signal Negative
HDMI_D0_P	IO34_L8P	W14	HDMI data 0 Positive
HDMI_D0_N	IO34_L8N	Y14	HDMI data 0 Negative
HDMI_D1_P	IO34_L17P	Y18	HDMI data 1 Positive
HDMI_D1_N	IO34_L17N	Y19	HDMI data 1 Negative
HDMI_D2_P	IO34_L7P	Y16	HDMI data 2 positive
HDMI_D2_N	IO34_L7N	Y17	HDMI data 2 Negative
HDMI_SCL	IO34_L21N	V18	HDMI IIC Clock
HDMI_SDA	IO34_L21P	V17	HDMI IIC Data

Part 3.9: MIPI camera interface (only for AX7Z020)

The AX7Z010 carrier board includes a MIPI camera interface, which can be used to connect with the ALINX Brand MIPI OV5640 camera module. The circuit schematic of the MIPI interface part is shown in Figure 3-9-1 below:

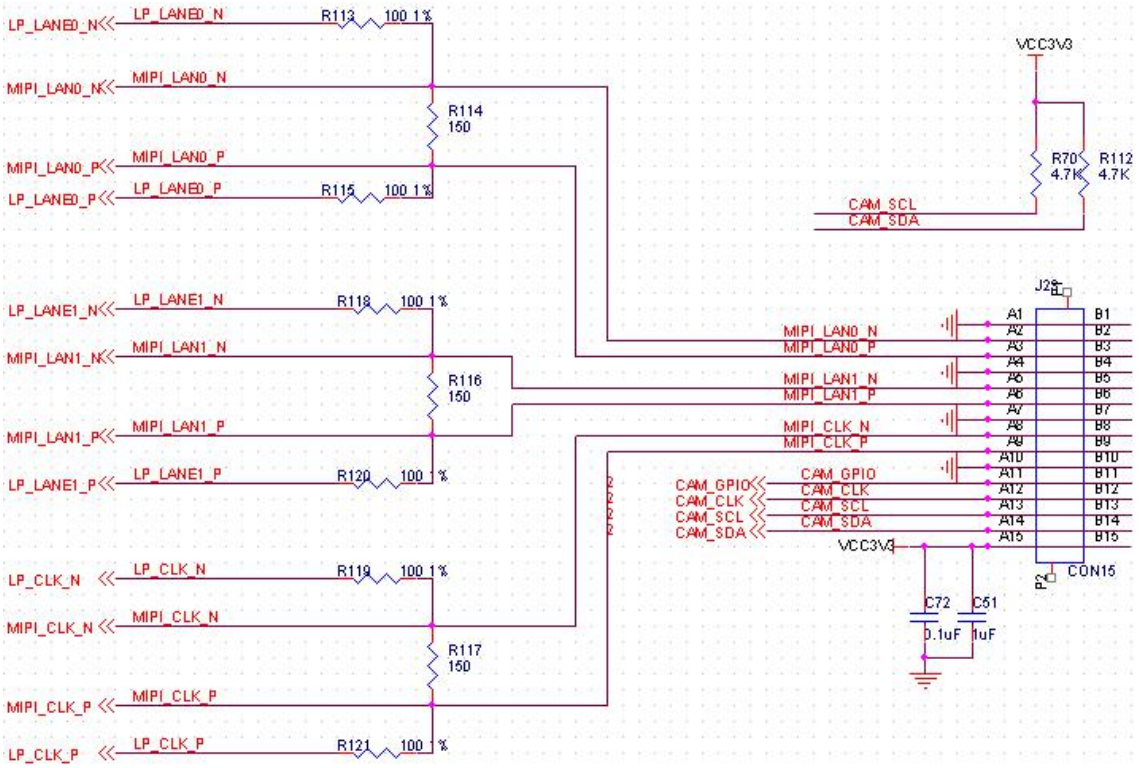


Figure 3-9-1: MIPI camera interface design schematic

Figure 3-9-2: MIPI camera interface on the carrier board

MIPI interface pin assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
LP_CLK_P	IO13_L15P	V8	Clock positive in Low Power Mode
LP_CLK_N	IO13_L15N	W8	Clock negative in Low Power Mode
LP_LANE0_P	IO13_L12P	T9	LANE0 positive in Low Power mode
LP_LANE0_N	IO13_L12N	U10	LANE0 negative in Low Power mode
LP_LANE1_P	IO13_L20P	Y12	LANE1 positive in Low Power mode
LP_LANE1_N	IO13_L20N	Y13	LANE1 negative in Low Power mode
MIPI_CLK_P	IO13_L13P	Y7	Clock positive in High Speed Mode
MIPI_CLK_N	IO13_L13N	Y6	Clock negative in High Speed Mode
MIPI_LAN0_P	IO13_L18P	W11	LANE0 positive in High Speed mode
MIPI_LAN0_N	IO13_L18N	Y11	LANE0 negative in High Speed mode
MIPI_LAN1_P	IO13_L17P	U9	LANE1 positive in High Speed mode
MIPI_LAN1_N	IO13_L17N	U8	LANE1 negative in High Speed mode
CAM_GPIO	IO13_L11P	U7	GPIO control of camera module
CAM_CLK	IO13_L11N	V7	Clock input of camera module
CAM_SCL	IO13_L19P	T5	I2C clock of camera module
CAM_SDA	IO13_L19N	U5	I2C data of camera module

Part 3.10: SD Card Slot Interface

The AX7Z010 FPGA Development Board contains a Micro SD card interface to provide user access to the SD card memory, the BOOT program for the ZYNQ chip, the Linux operating system kernel, the file system and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of ZYNQ. Since the VCCMIO of the BANK is set to 1.8V, but the data level of the SD card is 3.3V, connected through the TXS02612 level shifter. The schematic of the Zynq7000 PS and SD card connector is shown in Figure 3-10-1:

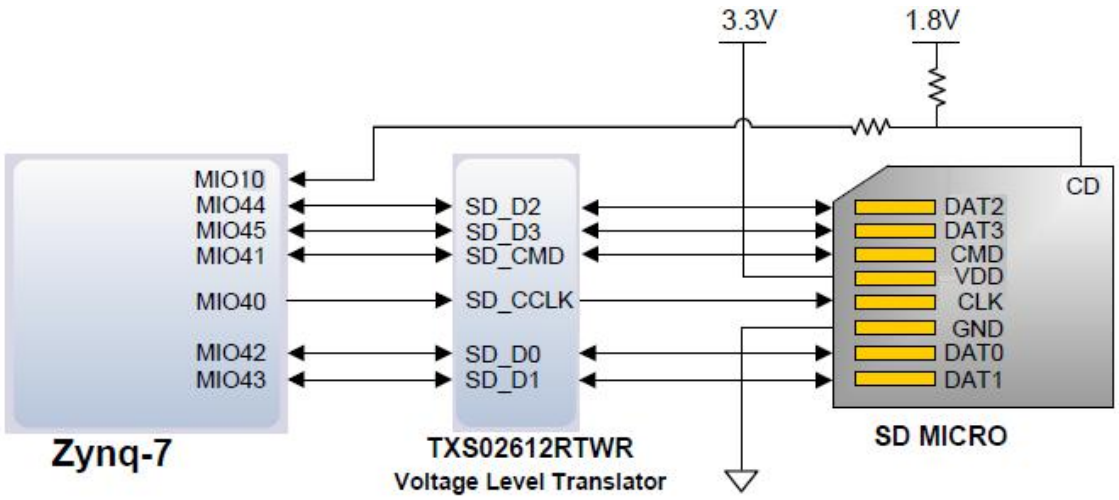


Figure 3-10-1: SD Card Connection Diagram

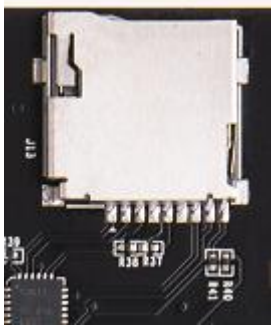


Figure 3-10-12: SD Card Interface on the carrier board

SD card slot pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
SD_CLK	PS_MIO40	D14	SD Clock Signal
SD_CMD	PS_MIO41	C17	SD Command Signal
SD_D0	PS_MIO42	E12	SD Data0
SD_D1	PS_MIO43	A9	SD Data1
SD_D2	PS_MIO44	F13	SD Data2
SD_D3	PS_MIO45	B15	SD Data3
SD_CD	PS_MIO47	B14	SD card insertion signal

Part 3.11: EEPROM

The AX7Z010 development board has an EEPROM onboard. The model of the EEPROM is 24LC04, and the capacity is: 4Kbit (2 * 256 * 8bit), which is composed of two 256byte blocks and communicates through the IIC bus. The on-board EEPROM is to learn the communication method of IIC bus. The I2C signal of EEPROM is connected to the I2C interface of the ZYNQ PS end. Figure 3-11-1 is the connection diagram of EEPROM

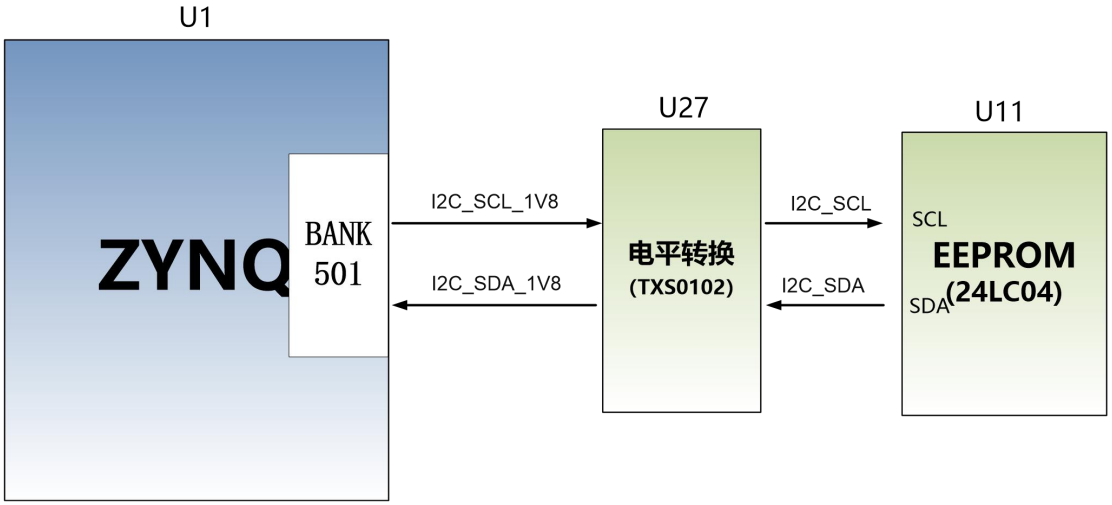


Figure 3-11-1: EEPROM connection diagram

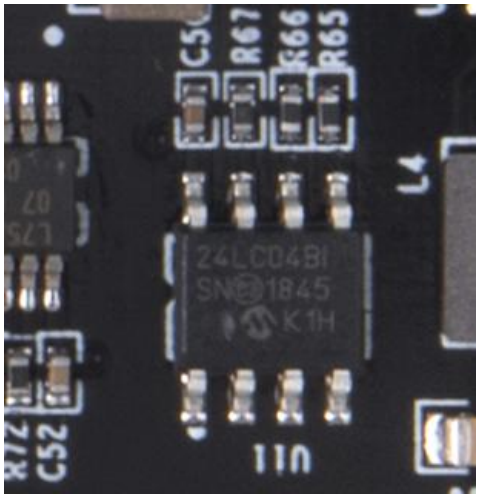


Figure 3-11-2: EEPROM on the carrier board

EEPROM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
I2C_SCL_1V8	MIO50	B13	IIC Clock Signal
I2C_SDA_1V8	MIO51	B9	IIC Data Signal

Part 3.12: Real-time clock

The FPGA development board has a real-time clock RTC chip, model DS1338, which provides the calendar function to 2099, year, month, day, minute, second, and week. If time is needed in the system, then RTC needs to be involved in the product. Externally need to connect a 32.768KHz passive clock, provide accurate clock source to the clock chip, so that RTC can accurately provide clock information to the product. At the same time, in order for the real-time clock to run normally after the product is powered off, an additional battery is usually required to power the clock chip. In Figure 3-12-2, BT1 is a battery holder. After we put the coin cell battery (**model CR1220, voltage is 3V**), when the system loses the battery, the coin cell battery can also power the DS1338. In this way, regardless of whether the product is powered, DS1302 Will run normally, without interruption, and can provide continuous time information. The interface signal of RTC and EEPORM are shared I2C bus. Figure 3-12-1 shows the connection of DS1338

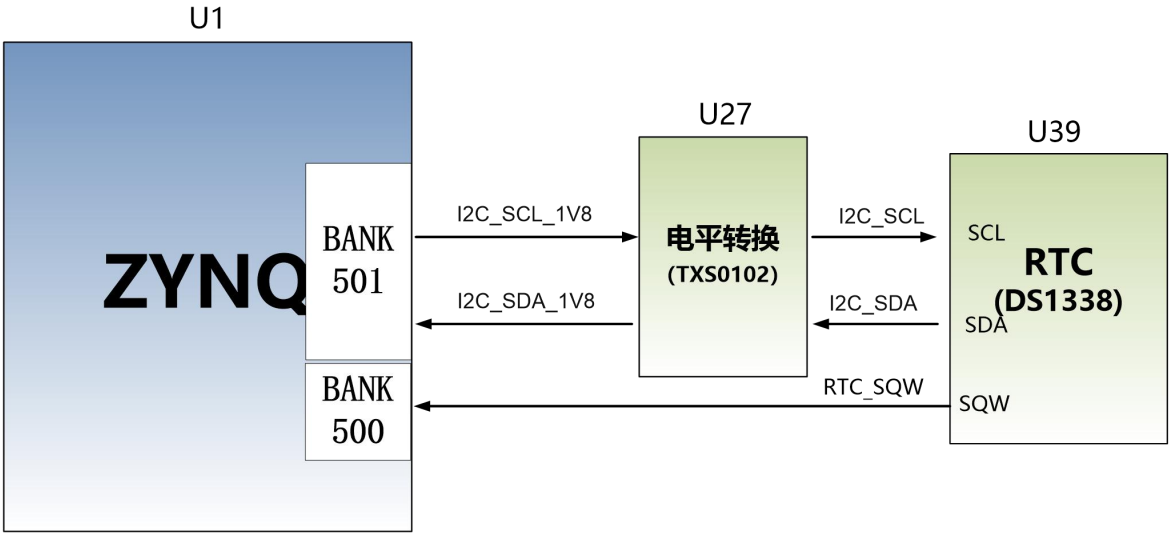


Figure 3-12-1: DS1338 Schematic

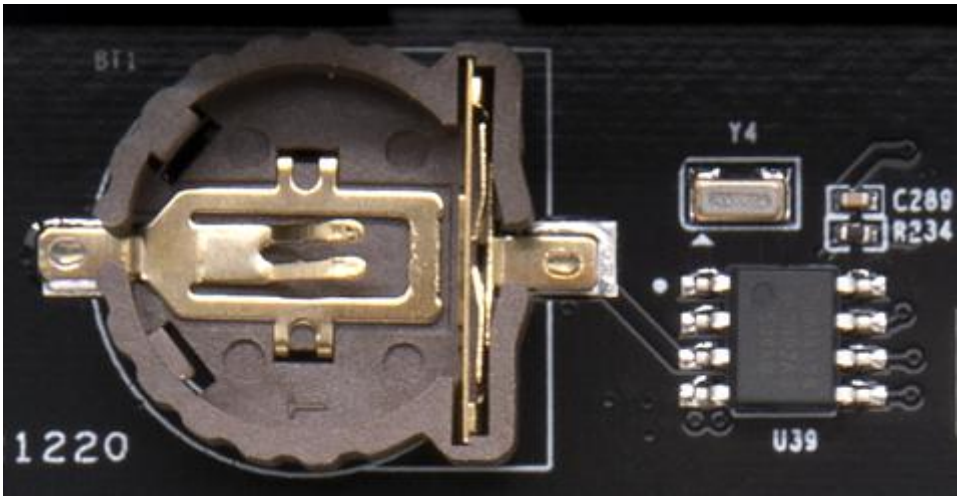


Figure 3-12-2: DS1338 on the carrier board

DS1338 interface pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
I2C_SCL_1V8	MIO50	B13	RTC Clock Signal
I2C_SDA_1V8	MIO51	B9	RTC reset signal
RTC_SQW	MIO7	D8	Square wave output signal

Part 3.13: Temperature sensor

A high-precision, low-power, digital temperature sensor chip is installed on the AX7Z010 development board, and the model is LM75 from ON

Semiconductor. The temperature accuracy of the LM75 chip is 0.5 degrees, and the sensor and FPGA are I2C digital interfaces. ZYNQ7010 reads the temperature near the current development board through the I2C interface. The interface signal of the LM75 sensor and EEPORM share the I2C bus. Figure 3-13-1 below shows the connection diagram of the LM75 sensor.

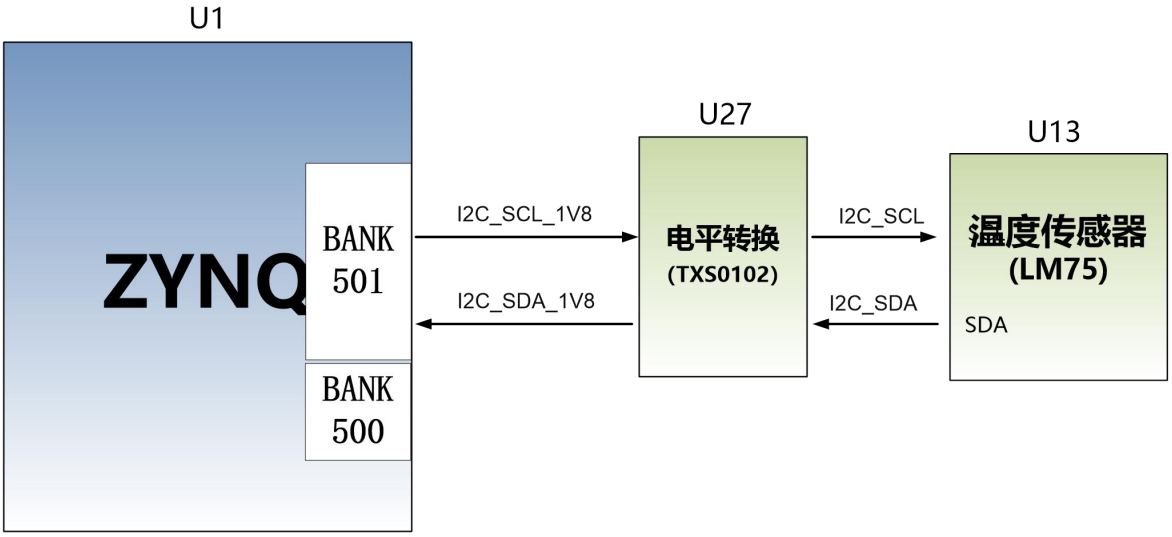


Figure 3-13-1: LM75 sensor connection diagram

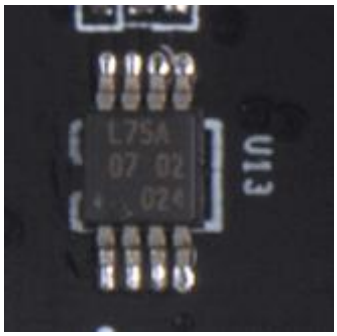


Figure 3-13-2: LM75 sensor on the AX7Z010 carrier board

Part 3.14: JTAG Debug Port

The JTAG download and debug circuit is reserved on the AX7Z010 carrier board, and the JTAG debug signals TCK, TDO, TMS, TDI of ZYNQ are derived. In order to prevent damage to the ZYNQ chip caused by hot plugging, a protection diode is added to the JTAG signal to ensure that the voltage of the

signal is within the range accepted by the FPGA to avoid damage of the ZYNQ chip.

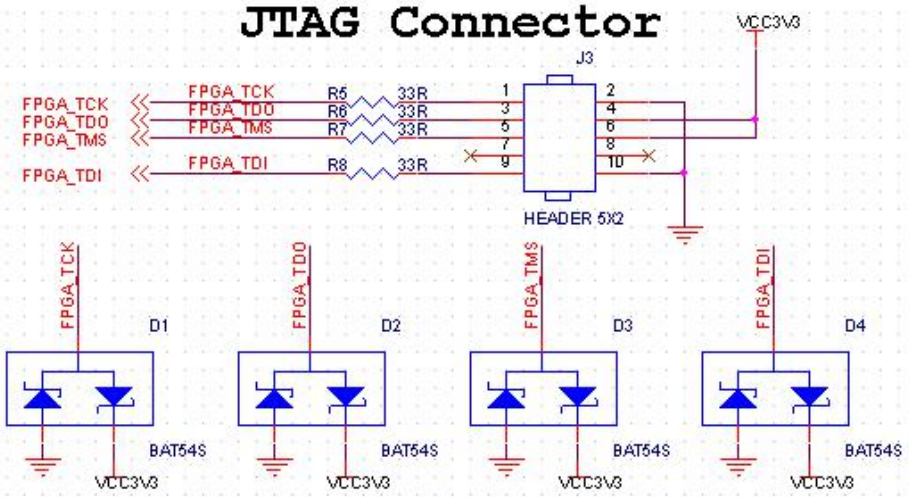


Figure 3-14-1: JTAG Interface Schematic

Users can connect the PC and JTAG interface to the ZYNQ system debugging through the USB cable provided by us. Be careful not to hot swap when JTAG cable is plugged and unplugged.

Figure 3-14-2: JTAG Interface on the Carrier Board

Part 3.15: User LEDs

The AX7Z010 has 4 LEDs on the carrier board, including 1 power indicator. The 4 user LED lights are all connected to the IO of the BANK35 on the PL side. The user can control the on and off through the program. When the IO voltage of the user LED light is high, the user LED light is off. When the connected IO voltage is low, the user LED will be lit. The LED light hardware connection

diagram is shown in Figure 3-15-1:

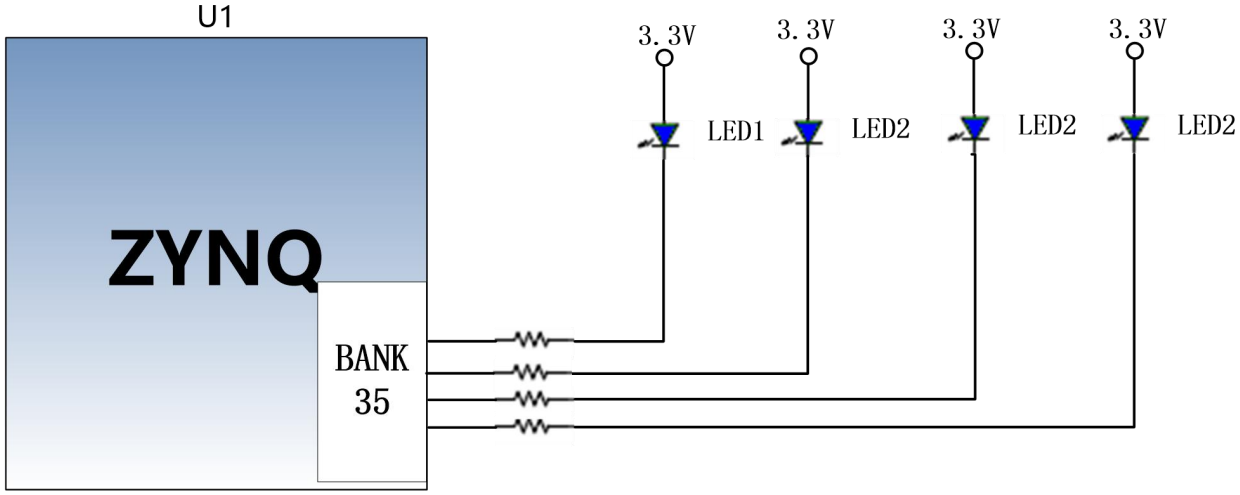


Figure 3-15-1: The User LEDs Hardware Connection Diagram

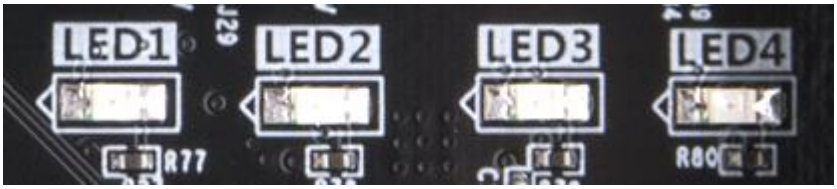


Figure 3-15-2: The User LEDs on the carrier board

Pin assignment of user LED lights

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
LED1	IO35_L20N	J14	User LED1
LED2	IO35_L20P	K14	User LED2
LED3	IO35_L14P	J18	User LED3
LED4	IO35_L14N	H18	User LED4

Part 3.16: User Keys

There are 4 user keys KEY1 ~ KEY4 on the AX7Z010 bottom plate, and the 4 user keys are connected to the IO of the BANK35 on the PL side. When the button is pressed, the signal is low. The ZYNQ chip detects a low level to determine whether the button is pressed. The diagram of user key connection is shown in Figure 3-16-1:

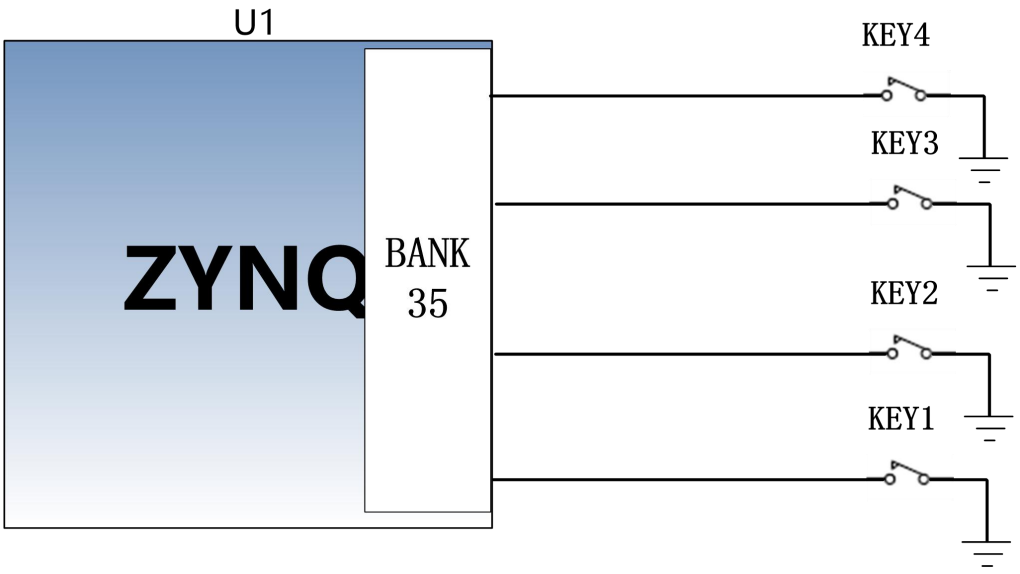


Figure 3-16-1: User keys connection diagram

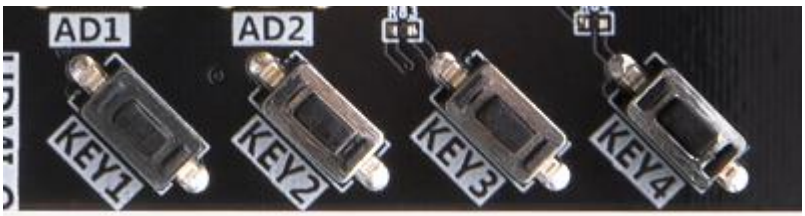


Figure 3-16-2: User keys on the carrier board

ZYNQ pin assignment of user keys

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
KEY1	IO35_L23N	M15	User KEY1
KEY2	IO35_L23P	M14	User KEY2
KEY3	IO35_L11N	L17	User KEY3
KEY4	IO35_L11P	L16	User KEY4

Part 3.17: Expansion Header

The carrier board is reserved with two 0.1-inch standard pitch 40-pin expansion ports J20 and J21, which are used to connect the ALINX modules or the external circuit designed by the user. The expansion port has 40 signals, of which 1-channel 5V power supply, 2-channel 3.3 V power supply, 3-channle ground and 34 IOs. **Do not directly connect the IO directly to the 5V device**

to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.

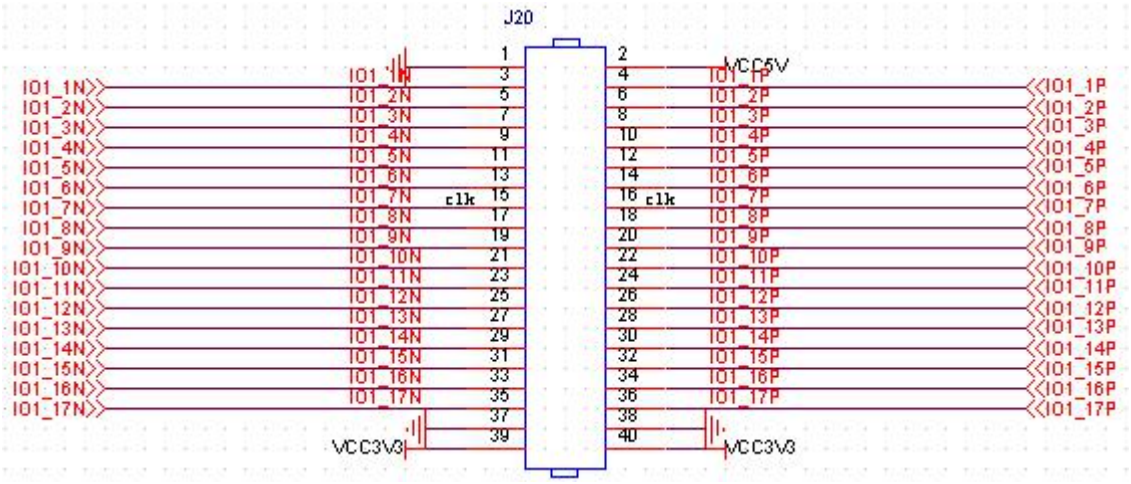


Figure 3-17-1: Expansion header J20 schematic

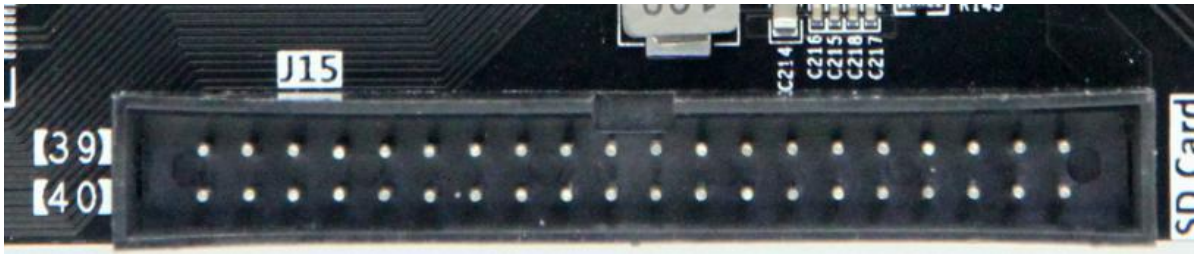


Figure 3-17-2: Expansion header J20 on the carrier board

J20 Expansion Header Pin Assignment

Pin Number	ZYNQ Pin	Pin Number	ZYNQ Pin
1	GND	**2**	+5V
3	R14	**4**	P14
5	U12	**6**	T12
7	T15	**8**	T14
9	T11	**10**	T10
11	U15	**12**	U14
13	P19	**14**	N18
15	R17	**16**	R16
17	P15	**18**	P16
19	N17	**20**	P18
21	V16	**22**	W16

23	R18	**24**	T17
25	W19	**26**	W18
27	W20	**28**	V20
29	P20	**30**	N20
31	U17	**32**	T16
33	U20	**34**	T20
35	V15	**36**	W15
37	GND	**38**	GND
39	+3.3V	**40**	+3.3V

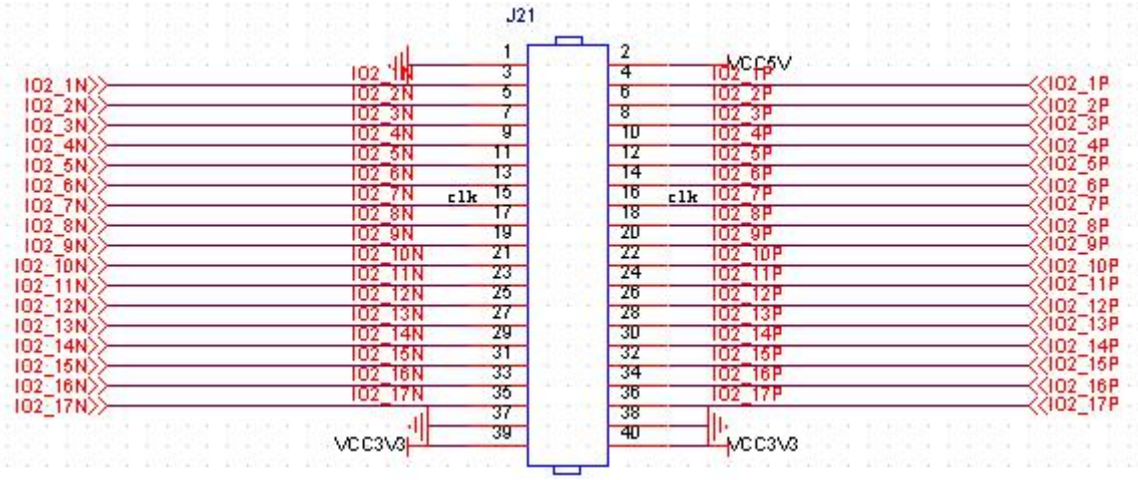


Figure 3-17-3: Expansion header J21 schematic

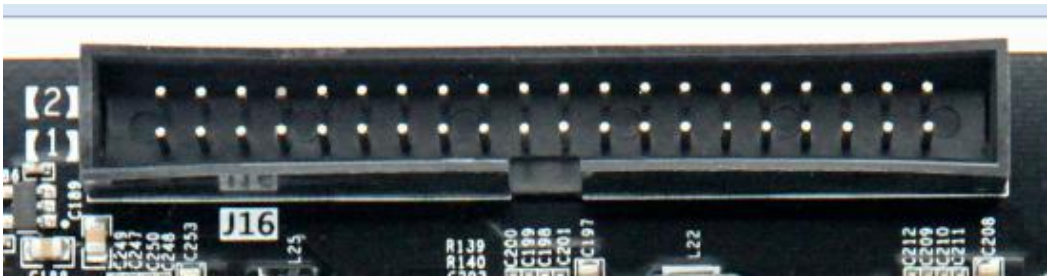


Figure 3-17-4: Expansion header J21 on the carrier board

J21 Expansion Header Pin Assignment

Pin Number	ZYNQ Pin	Pin Number	ZYNQ Pin
1	GND	**2**	+5V
3	M18	**4**	M17
5	K19	**6**	J19

7	B19	**8**	A20
9	B20	**10**	C20
11	G19	**12**	G20
13	M19	**14**	M20
15	D20	**16**	D19
17	L20	**18**	L19
19	F16	**20**	F17
21	H20	**22**	J20
23	G18	**24**	G17
25	H17	**26**	H16
27	G15	**28**	H15
29	K18	**30**	K17
31	J16	**32**	K16
33	N16	**34**	N15
35	L15	**36**	L14
37	GND	**38**	GND
39	+3.3V	**40**	+3.3V

Part 3.18: Power Supply

The power input voltage of the AX7Z010 FPGA development board is DC5V. On the carrier board, two DC / DC power chips TLV62130RGT and one LDO power chip SPX3819M5-ADJ are converted into three power sources of 1.8V, + 3.3V and VCCIO35. The default output of VCCIO35 is 3.3V. You can change the output of VCCIO35 by connecting a jumper to 2.5V or 1.8V.

The schematic diagram of the power supply design on the AX7Z010 FPGA carrier board is shown in Figure 3-18-1

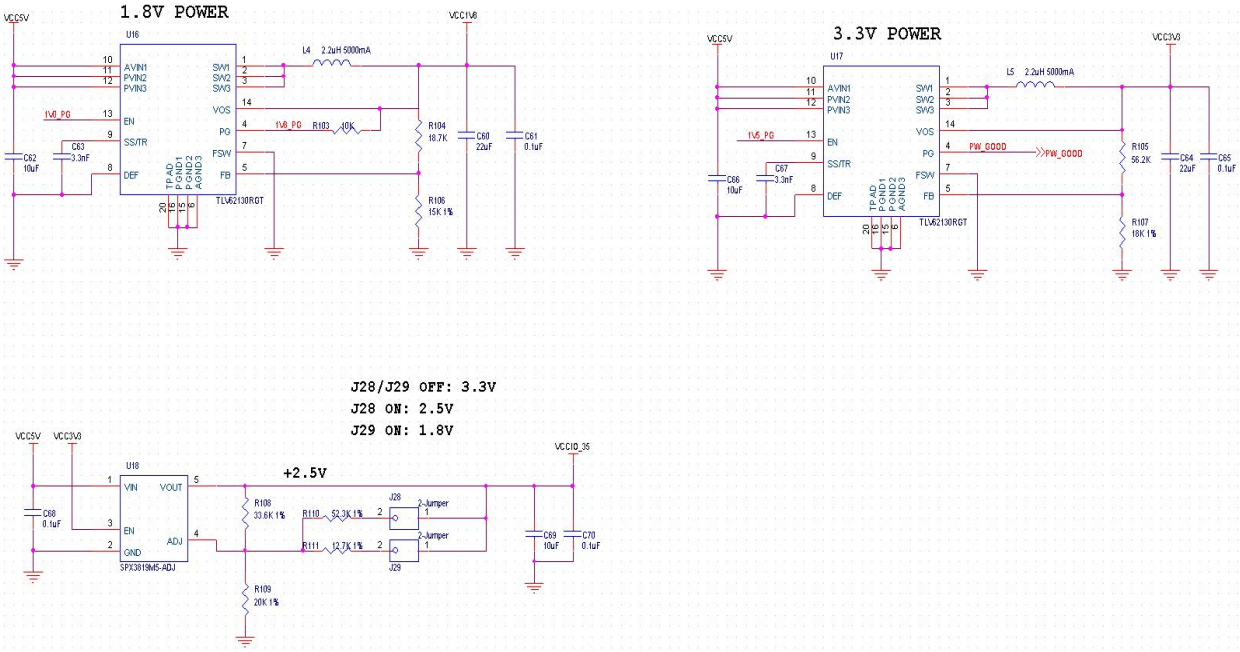


Figure 3-18-1: Carrier Board Power Schematic

The IO level of ZYNQ7010 BANK35 can be adjusted by the jumper cap on the carrier board. By default, if J28 and J29 are not equipped with jumper caps, the IO level of BANK35 is 3.3V. If a jumper cap is installed on J29, the IO level of BANK35 is 2.5V. If J28 is equipped with a jumper cap, the IO level of BANK35 is 1.8V.

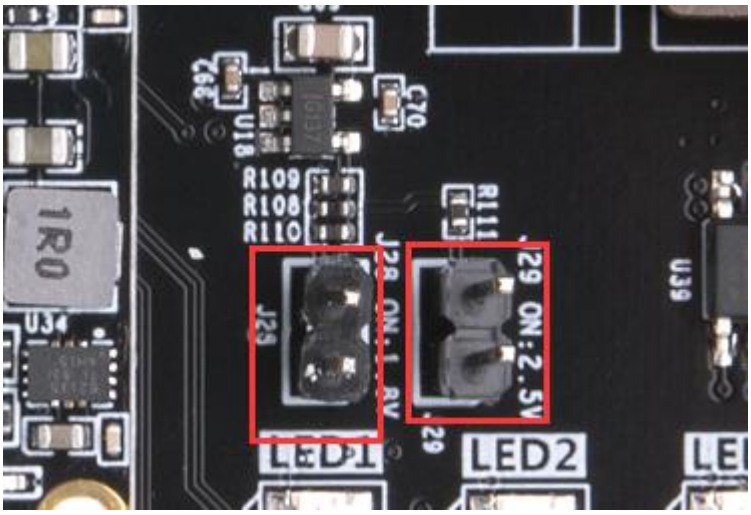


Figure 3-18-2: VCCIO35 voltage adjustment

Part 3.19: Carrier Board Size Dimension

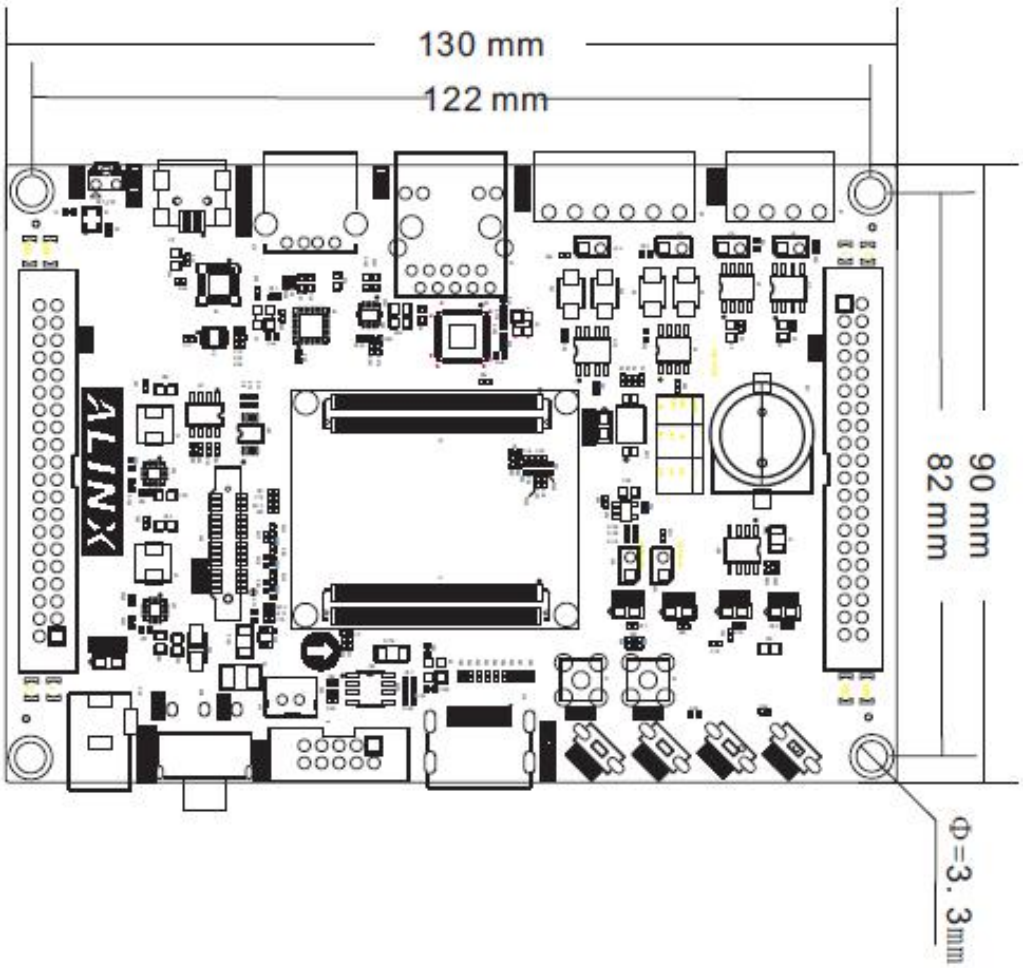


Figure 3-19-1: Top View