ZYNQ7000 FPGA Development Board AX7450

User Manual

Version Record

Revision	Date	Release By	Description
Rev 1.0	2020-11-21	Rachel Zhou	First Release

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The ZYNQ7000 FPGA development platform uses XILINX's Zynq7000 SOC chip XC7Z100 solution, which uses ARM+FPGA SOC technology to integrate dual-core ARM Cortex-A9 and FPGA programmable logic on a single chip. ZYNQ has two 512MB high-speed DDR3 SDRAM chips on the PS and four 512MB high-speed DDR3 SDRAM chips on the PL sides. In addition, there are one 8GB eMMC memory chip and two 256Mb QSPI FLASH chip on the PS side.

In terms of peripheral circuits, we have extended a wealth of interfaces for users, such as a PCIex8 slot, Gigabit Ethernet interfaces, 1 USB2.0 OTG interface, 1 UART serial interface, 1 SD card interface, 1 FMC HPC expansion interface, and 2 SMA interfaces etc. It meets users' requirements for high-speed data exchange, data storage, video transmission processing and industrial control. It is a "professional" ZYNQ development platform. For high-speed data transmission and exchange, pre-verification and post-application of data processing is possible. This product is very suitable for students, engineers and other groups engaged in ZYNQ development.

Part 1: FPGA Development Board Introduction

The AX7450 FPGA development board is mainly composed of ZYNQ7100 main chip, 6 DDR3, 1 eMMC, 2 QSPI FLASH and some peripheral interfaces. The ZYNQ7100 uses Xilinx's Zynq7000 series of chips, model number XC7Z100-2FFG900. The ZYNQ7100 chip can be divided into Processor System (PS) and Programmable Logic (PL). On the PS side of the ZYNQ7100 chip, there are two DDR3 chips and four DDR3 chips on the PL side. Each DDR3 has a capacity of up to 512M bytes, enabling the ARM system and FPGA system to independently process and store data. The 8GB eMMC FLASH memory chip on the PS side and two 256Mb QSPI FLASH are used to statically store ZYNQ's operating system, file system and user data.

The AX7450 FPGA development board expands its rich peripheral interface, including one PCIex8 slot, one Gigabit Ethernet interfaces, one USB2.0 OTG interfaces, one UART serial interface, one SD card interface, one FMC expansion interface, two SMT interfaces, some keys and LEDs.

Figure 1-1 is the Schematic diagram of the entire FPGA development boards:

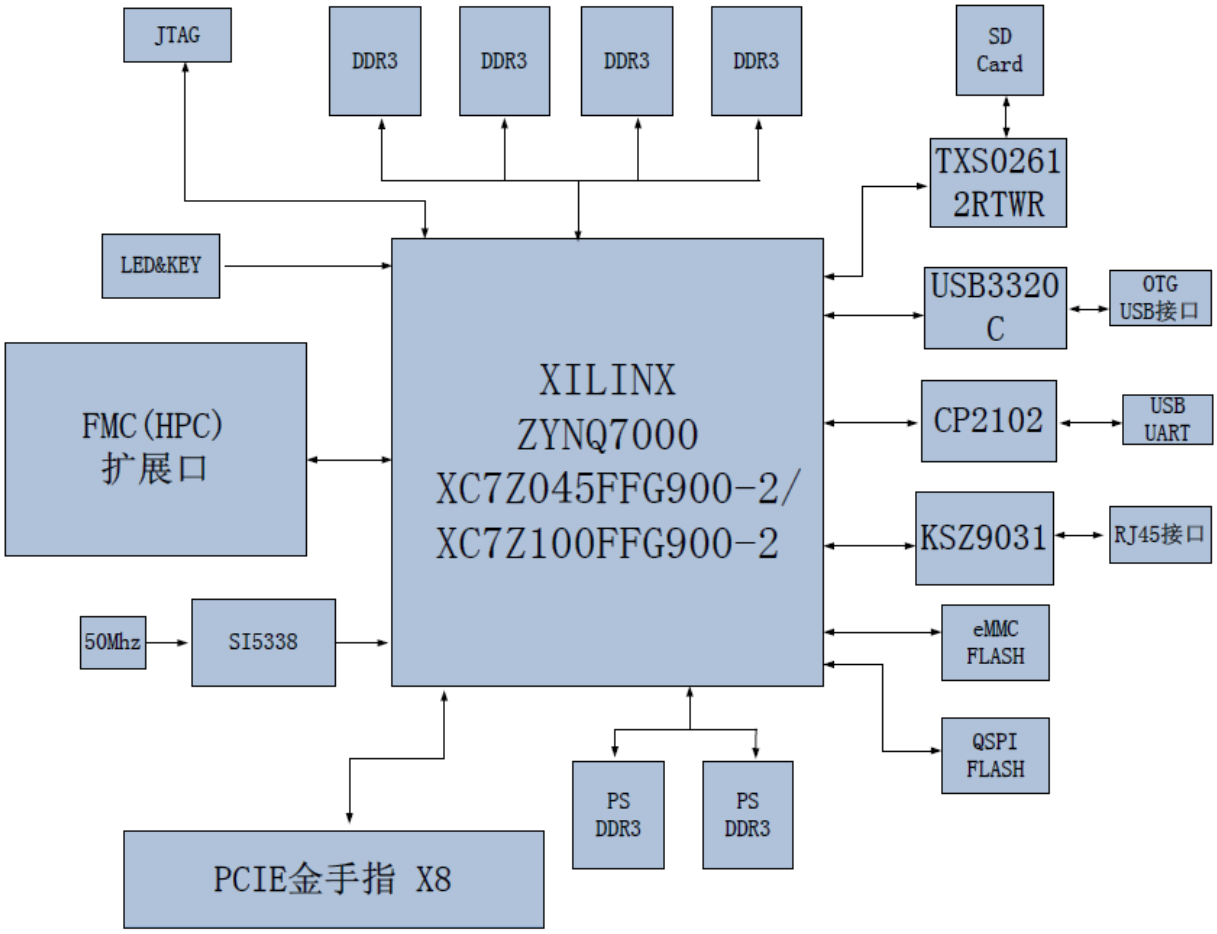


Figure 1-1: The Schematic Diagram of the AX7450

Through this diagram, you can see the interfaces and functions that the AX7450 FPGA Development Board contains:

- Xilinx ARM+FPGA chip Zynq-7000 XC7Z100-2FFG900
- DDR3

  With 6 large-capacity 512M bytes (3GB total), high-speed DDR3 SDRAM. Two of them are mounted on the PS side to form a 32-bit data width, which can be used as a cache for ZYNQ chip data, or as a memory for operating system operation; the other 4 are mounted on the PL side to form a 64-bit data width and can be used as an FPGA Data storage, image analysis cache, data processing.
- eMMC

  The PS side mounts an 8GB eMMC FLASH memory chip to store user

operating system files or other user data.

- QSPI FLASH

  Two 256Mbit QSPI FLASH memory chip can be used as a Uboot file for ZYNQ chips, storage of system files and user data;

- PCIe Interface

  Support PCI Express 2.0 standard, provide standard PCIe x8 high-speed data transmission interface, single channel communication rate can be as high as 5GBaud

- Gigabite Ethernet Interface

  10/100M/1000M Ethernet RJ45 interface for Ethernet data exchange with computers or other network devices. The network interface chip uses Micrel's KSZ9031 industrial grade GPHY chip, connected to the PS end of the ZYNQ chip.

- USB2.0 Interface

  It is used for OTG communication with PC or USB device, the connector adopts MINI USB interface.

- USB Uart Interface

  Uart to USB interfaces for communication with the computer, for user debugging, and the USB interface adopts the MINI USB interface.

- Micro SD card holder

  1-channel Micro SD card holder, for save operating system images and file systems.

- FMC HPC expansion port

  A standard FMC HPC expansion port for connecting XILINX or ALINXDE various FMC modules (HDMI input and output modules, binocular camera modules, high-speed AD modules etc.). The FMC expansion port contains 84 pairs of differential IO signals and 8 high-speed GTX transceiver signals.

- USB JTAG Interface

One way USB JTAG port, debug and download ZYNQ system through USB cable and onboard JTAG circuit

- SMA Interface

  2 SMA interfaces, users can connect external trigger signals or clock signals.

- Clock

  An on-board 33.333Mhz active crystal oscillator provides a stable clock source for the PS system, a 50MHz active crystal oscillator that provides additional clocking for the PL logic, and a programmable clock chip on the board that provides the clock source for the GTX. Provide a reference clock for PCIE, SFP and DDR operation.

- LED Light

  7 LEDs, 1 power indicator; 1 DONE configuration indicator; 4 user debugging LED lights, 1 front panel dual-color LED light.

- Keys

  2 keys, 1 reset key , 1 PL user key.

Part 2: ZYNQ Chip

The AX7450 FPGA development board uses Xilinx's Zynq7000 series chip, model XC7Z100-2FFG900. The chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO etc. The PS can operate independently and start up at power up or reset. Figure 2-1 detailed the Overall Block Diagram of the ZYNQ7000 Chip.

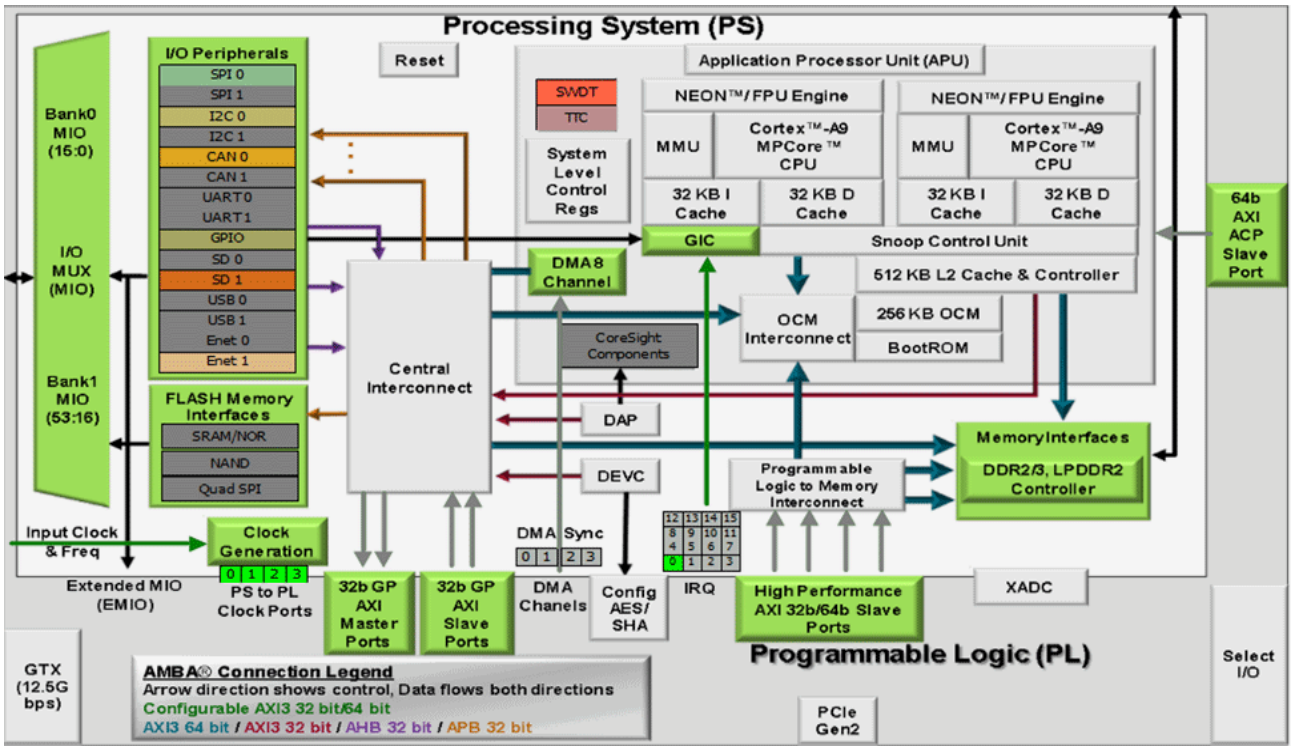


Figure 2-1: Overall Block Diagram of the ZYNQ7000 Chip

The main parameters of the PS system part are as follows:

- ARM dual-core CortexA9-based application processor, ARM-v7 architecture, up to 800MHz
- 32KB level 1 instruction and data cache per CPU, 512KB level 2 cache

2 CPU shares

- On-chip boot ROM and 256KB on-chip RAM
- External storage interface, support 16/32 bit DDR2, DDR3 interface
- Two Gigabit NIC support: divergent-aggregate DMA, GMII, RGMII, SGMII interface
- Two USB2.0 OTG interfaces, each supporting up to 12 nodes
- Two CAN2.0B bus interfaces
- Two SD card, SDIO, MMC compatible controllers
- 2 SPIs, 2 UARTs, 2 I2C interfaces
- 54 multi-function IOs that can be configured as normal IO or peripheral control interfaces
- High bandwidth connection within PS and PS to PL

The main parameters of the PL logic part are as follows:

- Logic Cells: 444K
- Look-up-tables (LUTs): 277,400
- Flip-flops: 554,800
- 18x25MACCs：2020
- Block RAM：26.5 Mb
- 16-channel high-speed GTX transceiver, supporting PCIE Gen2x8;
- Two AD converters for on-chip voltage, temperature sensing and up to 17 external differential input channels, 1MBPS

XC7Z100-2FFG900I chip speed grade is -2, industrial grade, package is FGG900, pin pitch is 1.0mm the specific chip model definition of ZYNQ7000 series is shown in Figure 2-2

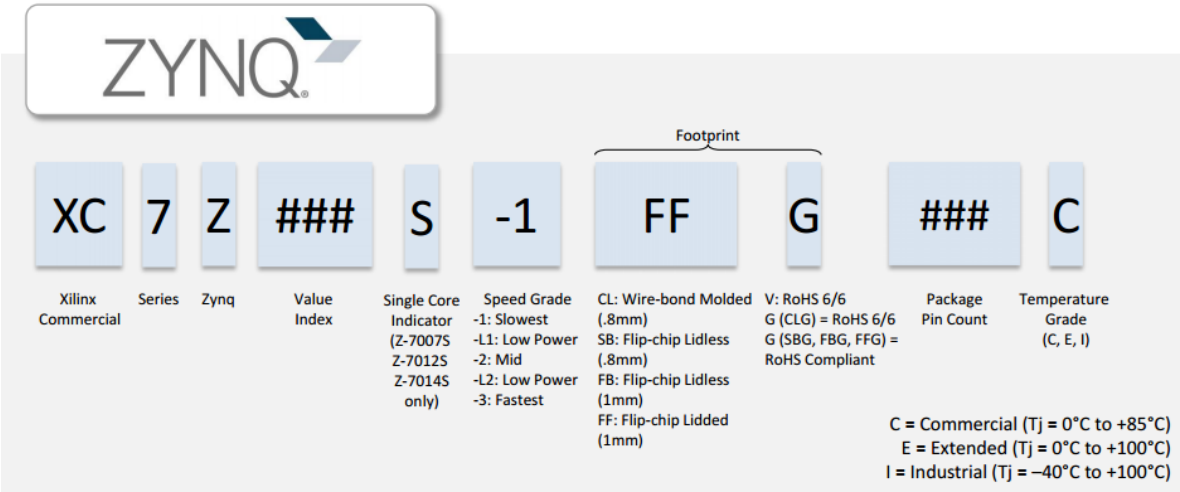


Figure 2-2: The Specific Chip Model Definition of ZYNQ7000 Series

Figure 2-3: The XC7Z100 chip used on the Core Board

Part 3: DDR3 DRAM

The AX7450 FPGA development board is equipped with 6 Micron (Micron) 512MB DDR3 chips, model MT41J256M16HA-125 (compatible with MT41K256M16HA-125). The PS mounts 2 slices to form a 32-bit data width, and the PL end mounts 4 slices to form a 64-bit data width. The DDR3 SDRAM on the PS side can run at a maximum speed of 533MHz (data rate 1066Mbps), and two DDR3 storage systems are directly connected to the memory interface of the BANK 502 of the ZYNQ processing system (PS). The maximum operating speed of DDR3 SDRAM on the PL side can reach 800MHz (data rate 1600Mbps), and four DDR3 storage systems are connected to the BANK33 and BANK34 interfaces of the FPGA. The specific configuration of DDR3 SDRAM is shown in Table 3-1.

Bit Number	Chip Model	Capacity	Factory
U5,U6,U8,U9,U11,U12	MT41J256M16HA-125	256M x 16bit	Micron

Table 3-1: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

The hardware connection of the DDR3 DRAM on the PS side is shown in Figure 3-1:

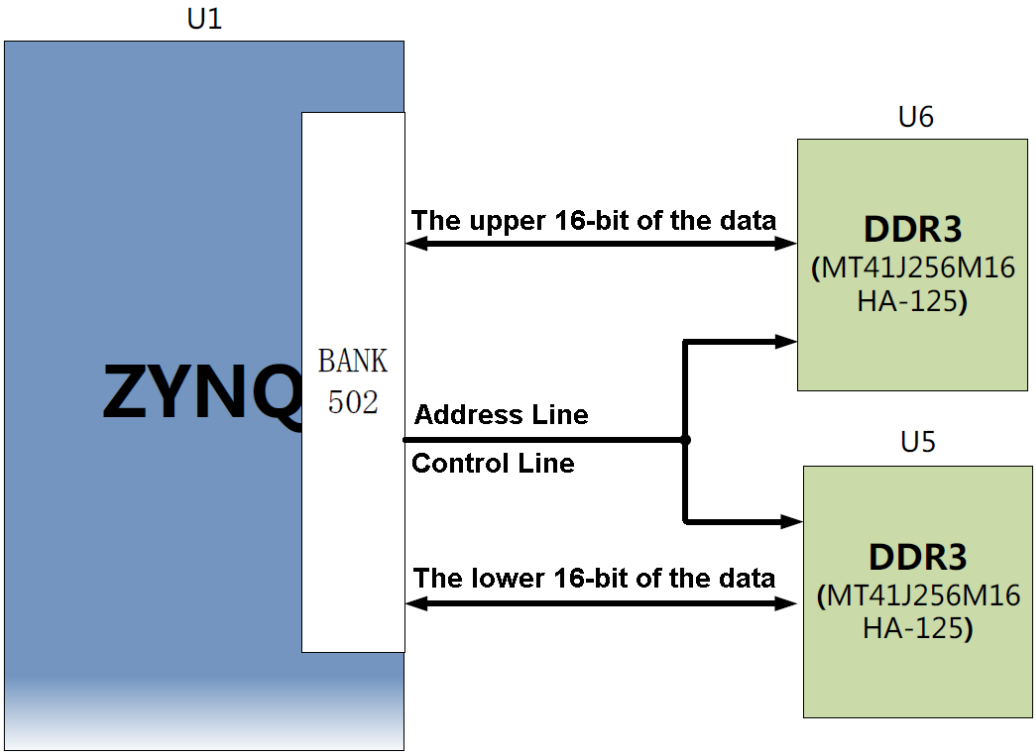


Figure 3-1: The Schematic Part of DDR3 DRAM on the PS side

The hardware connection of DDR3 DRAM on the PL side is shown in Figure 3-2:

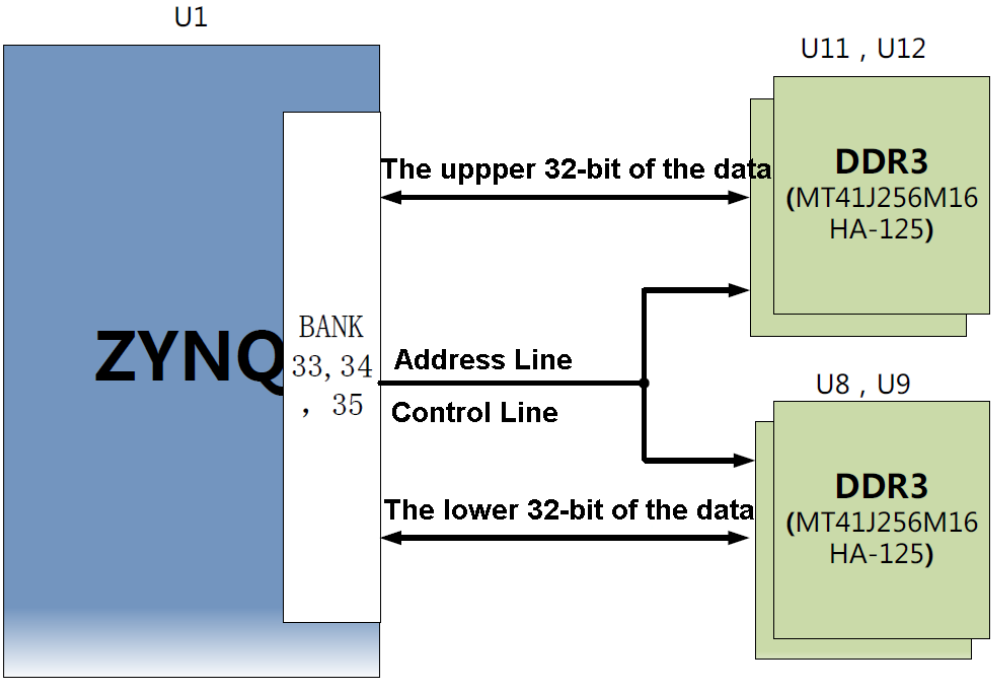


Figure 3-2: The Schematic Part of DDR3 DRAM on the PL side

PS side DDR3 DRAM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
PS_DDR3_DQS0_P	PS_DDR_DQS_P0_502	C26
PS_DDR3_DQS0_N	PS_DDR_DQS_N0_502	B26
PS_DDR3_DQS1_P	PS_DDR_DQS_P1_502	C29
PS_DDR3_DQS1_N	PS_DDR_DQS_N1_502	B29
PS_DDR3_DQS2_P	PS_DDR_DQS_P2_502	G29
PS_DDR3_DQS2_N	PS_DDR_DQS_N2_502	F29
PS_DDR3_DQS3_P	PS_DDR_DQS_P3_502	L28
PS_DDR3_DQS4_N	PS_DDR_DQS_N3_502	L29
PS_DDR3_D0	PS_DDR_DQ0_502	A25
PS_DDR3_D1	PS_DDR_DQ1_502	E25
PS_DDR3_D2	PS_DDR_DQ2_502	B27
PS_DDR3_D3	PS_DDR_DQ3_502	D25
PS_DDR3_D4	PS_DDR_DQ4_502	B25
PS_DDR3_D5	PS_DDR_DQ5_502	E26
PS_DDR3_D6	PS_DDR_DQ6_502	D26
PS_DDR3_D7	PS_DDR_DQ7_502	E27
PS_DDR3_D8	PS_DDR_DQ8_502	A29
PS_DDR3_D9	PS_DDR_DQ9_502	A27
PS_DDR3_D10	PS_DDR_DQ10_502	A30
PS_DDR3_D11	PS_DDR_DQ11_502	A28
PS_DDR3_D12	PS_DDR_DQ12_502	C28
PS_DDR3_D13	PS_DDR_DQ13_502	D30
PS_DDR3_D14	PS_DDR_DQ14_502	D28
PS_DDR3_D15	PS_DDR_DQ15_502	D29
PS_DDR3_D16	PS_DDR_DQ16_502	H27
PS_DDR3_D17	PS_DDR_DQ17_502	G27
PS_DDR3_D18	PS_DDR_DQ18_502	H28
PS_DDR3_D19	PS_DDR_DQ19_502	E28
PS_DDR3_D20	PS_DDR_DQ20_502	E30
PS_DDR3_D21	PS_DDR_DQ21_502	F28
PS_DDR3_D22	PS_DDR_DQ22_502	G30
PS_DDR3_D23	PS_DDR_DQ23_502	F30

PS_DDR3_D24	PS_DDR_DQ24_502	J29
PS_DDR3_D25	PS_DDR_DQ25_502	K27
PS_DDR3_D26	PS_DDR_DQ26_502	J30
PS_DDR3_D27	PS_DDR_DQ27_502	J28
PS_DDR3_D28	PS_DDR_DQ28_502	K30
PS_DDR3_D29	PS_DDR_DQ29_502	M29
PS_DDR3_D30	PS_DDR_DQ30_502	L30
PS_DDR3_D31	PS_DDR_DQ31_502	M30
PS_DDR3_DM0	PS_DDR_DM0_502	C27
PS_DDR3_DM1	PS_DDR_DM1_502	B30
PS_DDR3_DM2	PS_DDR_DM2_502	H29
PS_DDR3_DM3	PS_DDR_DM3_502	K28
PS_DDR3_A0	PS_DDR_A0_502	L25
PS_DDR3_A1	PS_DDR_A1_502	K26
PS_DDR3_A2	PS_DDR_A2_502	L27
PS_DDR3_A3	PS_DDR_A3_502	G25
PS_DDR3_A4	PS_DDR_A4_502	J26
PS_DDR3_A5	PS_DDR_A5_502	G24
PS_DDR3_A6	PS_DDR_A6_502	H26
PS_DDR3_A7	PS_DDR_A7_502	K22
PS_DDR3_A8	PS_DDR_A8_502	F27
PS_DDR3_A9	PS_DDR_A9_502	J23
PS_DDR3_A10	PS_DDR_A10_502	G26
PS_DDR3_A11	PS_DDR_A11_502	H24
PS_DDR3_A12	PS_DDR_A12_502	K23
PS_DDR3_A13	PS_DDR_A13_502	H23
PS_DDR3_A14	PS_DDR_A14_502	J24
PS_DDR3_BA0	PS_DDR_BA0_502	M27
PS_DDR3_BA1	PS_DDR_BA1_502	M26
PS_DDR3_BA2	PS_DDR_BA2_502	M25
PS_DDR3_S0	PS_DDR_CS_B_502	N22
PS_DDR3_RAS	PS_DDR_RAS_B_502	N24
PS_DDR3_CAS	PS_DDR_CAS_B_502	M24

PS_DDR3_WE	PS_DDR_WE_B_502	N23
PS_DDR3_ODT	PS_DDR_ODT_502	L23
PS_DDR3_RESET	PS_DDR_DRST_B_502	F25
PS_DDR3_CLK0_P	PS_DDR_CKP_502	K25
PS_DDR3_CLK0_N	PS_DDR_CKN_502	J25
PS_DDR3_CKE	PS_DDR_CKE_502	M22

PL side DDR3 DRAM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
PL_DDR3_DM0	IO_L4P_T0_35	J14
PL_DDR3_DQS0_N	IO_L3N_T0_DQS_AD1N_35	K13
PL_DDR3_DQS0_P	IO_L3P_T0_DQS_AD1P_35	L13
PL_DDR3_D0	IO_L5N_T0_AD9N_35	J15
PL_DDR3_D1	IO_L2N_T0_AD8N_35	H13
PL_DDR3_D2	IO_L1P_T0_AD0P_35	L15
PL_DDR3_D3	IO_L2P_T0_AD8P_35	J13
PL_DDR3_D4	IO_L5P_T0_AD9P_35	K15
PL_DDR3_D5	IO_L1N_T0_AD0N_35	L14
PL_DDR3_D6	IO_L6P_T0_35	J16
PL_DDR3_D7	IO_L4N_T0_35	H14
PL_DDR3_DM1	IO_L12N_T1_MRCC_35	F14
PL_DDR3_DQS1_N	IO_L9N_T1_DQS_AD3N_35	F12
PL_DDR3_DQS1_P	IO_L9P_T1_DQS_AD3P_35	G12
PL_DDR3_D8	IO_L8N_T1_AD10N_35	G14
PL_DDR3_D9	IO_L10N_T1_AD11N_35	E12
PL_DDR3_D10	IO_L7N_T1_AD2N_35	G16
PL_DDR3_D11	IO_L11N_T1_SRCC_35	D13
PL_DDR3_D12	IO_L10P_T1_AD11P_35	F13
PL_DDR3_D13	IO_L11P_T1_SRCC_35	E13
PL_DDR3_D14	IO_L8P_T1_AD10P_35	G15
PL_DDR3_D15	IO_L12P_T1_MRCC_35	F15
PL_DDR3_DM2	IO_L16N_T2_35	C16
PL_DDR3_DQS2_N	IO_L15N_T2_DQS_AD12N_35	E17
PL_DDR3_DQS2_P	IO_L15P_T2_DQS_AD12P_35	F17
PL_DDR3_D16	IO_L18N_T2_AD13N_35	A17

PL_DDR3_D17	IO_L16P_T2_35	D16
PL_DDR3_D18	IO_L17P_T2_AD5P_35	C17
PL_DDR3_D19	IO_L14P_T2_AD4P_SRCC_35	D15
PL_DDR3_D20	IO_L17N_T2_AD5N_35	B16
PL_DDR3_D21	IO_L13N_T2_MRCC_35	E15
PL_DDR3_D22	IO_L18P_T2_AD13P_35	B17
PL_DDR3_D23	IO_L14N_T2_AD4N_SRCC_35	D14
PL_DDR3_DM3	IO_L20P_T3_AD6P_35	C12
PL_DDR3_DQS3_N	IO_L21N_T3_DQS_AD14N_35	A15
PL_DDR3_DQS3_P	IO_L21P_T3_DQS_AD14P_35	B15
PL_DDR3_D24	IO_L22P_T3_AD7P_35	C11
PL_DDR3_D25	IO_L23P_T3_35	B14
PL_DDR3_D26	IO_L22N_T3_AD7N_35	B11
PL_DDR3_D27	IO_L24N_T3_AD15N_35	A12
PL_DDR3_D28	IO_L24P_T3_AD15P_35	A13
PL_DDR3_D29	IO_L19P_T3_35	C14
PL_DDR3_D30	IO_L20N_T3_AD6N_35	B12
PL_DDR3_D31	IO_L23N_T3_35	A14
PL_DDR3_DM4	IO_L2P_T0_33	L1
PL_DDR3_DQS4_N	IO_L3N_T0_DQS_33	K2
PL_DDR3_DQS4_P	IO_L3P_T0_DQS_33	K3
PL_DDR3_D32	IO_L1N_T0_33	J3
PL_DDR3_D33	IO_L4N_T0_33	L2
PL_DDR3_D34	IO_L1P_T0_33	J4
PL_DDR3_D35	IO_L4P_T0_33	L3
PL_DDR3_D36	IO_L2N_T0_33	K1
PL_DDR3_D37	IO_L6P_T0_33	K6
PL_DDR3_D38	IO_L5N_T0_33	J5
PL_DDR3_D39	IO_L5P_T0_33	K5
PL_DDR3_DM5	IO_L12P_T1_MRCC_33	G5
PL_DDR3_DQS5_N	IO_L9N_T1_DQS_33	H1
PL_DDR3_DQS5_P	IO_L9P_T1_DQS_33	J1
PL_DDR3_D40	IO_L11P_T1_SRCC_33	H4
PL_DDR3_D41	IO_L10N_T1_33	G1
PL_DDR3_D42	IO_L8P_T1_33	H6
PL_DDR3_D43	IO_L7N_T1_33	F2

PL_DDR3_D44	IO_L10P_T1_33	H2
PL_DDR3_D45	IO_L12N_T1_MRCC_33	G4
PL_DDR3_D46	IO_L8N_T1_33	G6
PL_DDR3_D47	IO_L11N_T1_SRCC_33	H3
PL_DDR3_DM6	IO_L14N_T2_SRCC_33	F3
PL_DDR3_DQS6_N	IO_L15N_T2_DQS_33	D5
PL_DDR3_DQS6_P	IO_L15P_T2_DQS_33	E6
PL_DDR3_D48	IO_L18P_T2_33	E1
PL_DDR3_D49	IO_L17P_T2_33	E3
PL_DDR3_D50	IO_L16N_T2_33	D3
PL_DDR3_D51	IO_L14P_T2_SRCC_33	F4
PL_DDR3_D52	IO_L18N_T2_33	D1
PL_DDR3_D53	IO_L13N_T2_MRCC_33	E5
PL_DDR3_D54	IO_L16P_T2_33	D4
PL_DDR3_D55	IO_L17N_T2_33	E2
PL_DDR3_DM7	IO_L23N_T3_33	B1
PL_DDR3_DQS7_N	IO_L21N_T3_DQS_33	A4
PL_DDR3_DQS7_P	IO_L21P_T3_DQS_33	A5
PL_DDR3_D56	IO_L22P_T3_33	C2
PL_DDR3_D57	IO_L24N_T3_33	A2
PL_DDR3_D58	IO_L20N_T3_33	B4
PL_DDR3_D59	IO_L20P_T3_33	B5
PL_DDR3_D60	IO_L22N_T3_33	C1
PL_DDR3_D61	IO_L24P_T3_33	A3
PL_DDR3_D62	IO_L19P_T3_33	C4
PL_DDR3_D63	IO_L23P_T3_33	B2
PL_DDR3_A14	IO_L22N_T3_34	K10
PL_DDR3_A13	IO_L7P_T1_34	J11
PL_DDR3_A12	IO_L13P_T2_MRCC_34	H9
PL_DDR3_A11	IO_L20N_T3_34	J9
PL_DDR3_A10	IO_L18N_T2_34	G7
PL_DDR3_A9	IO_L9P_T1_DQS_34	H12
PL_DDR3_A8	IO_L23P_T3_34	L10
PL_DDR3_A7	IO_L10P_T1_34	E10
PL_DDR3_A6	IO_L19P_T3_34	L7
PL_DDR3_A5	IO_L8N_T1_34	D11

PL_DDR3_A4	IO_L15N_T2_DQS_34	H8
PL_DDR3_A3	IO_L10N_T1_34	D10
PL_DDR3_A2	IO_L7N_T1_34	H11
PL_DDR3_A1	IO_L21P_T3_DQS_34	L8
PL_DDR3_A0	IO_L18P_T2_34	H7
PL_DDR3_BA2	IO_L9N_T1_DQS_34	G11
PL_DDR3_BA1	IO_L21N_T3_DQS_34	K8
PL_DDR3_BA0	IO_L22P_T3_34	K11
PL_DDR3_CLK0_P	IO_L12P_T1_MRCC_34	D9
PL_DDR3_CLK0_N	IO_L12N_T1_MRCC_34	D8
PL_DDR3_RAS	IO_L13N_T2_MRCC_34	G9
PL_DDR3_S0	IO_L16P_T2_34	F8
PL_DDR3_WE	IO_L16N_T2_34	F7
PL_DDR3_CAS	IO_L17P_T2_34	E7
PL_DDR3_CKE	IO_L17N_T2_34	D6
PL_DDR3_ODT	IO_L20P_T3_34	J10
PL_DDR3_RESET	IO_L8P_T1_34	E11

Part 4: QSPI Flash

The AX7450 FPGA development board is equipped with two 256MBit Quad-SPI FLASH chip, model W25Q256FVEI, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 4-1.

Position	Model	Capacity	Factory
U13,U14	W25Q256FVEI	32M Byte	Winbond

Table 4-1: QSPI FLASH Specification

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 4-1 shows the QSPI Flash in the schematic.

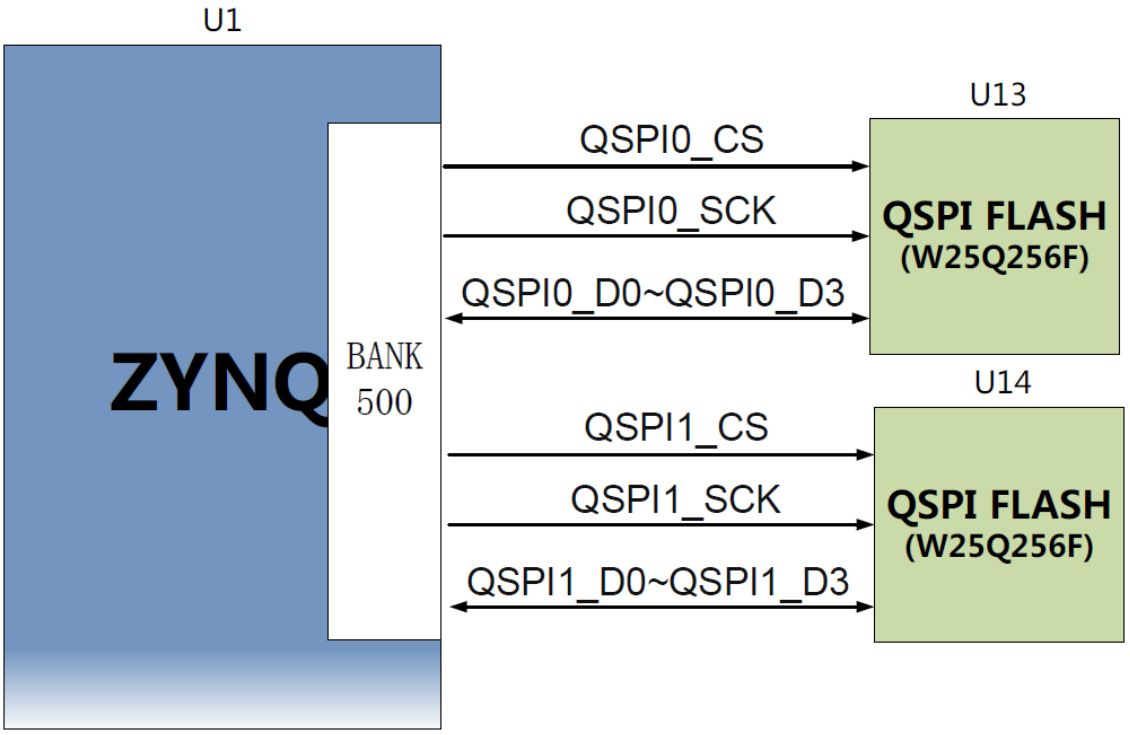


Figure 4-1: QSPI Flash in the schematic

Configure chip pin assignments:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
QSPI0_SCK	PS_MIO6_500	D24
QSPI0_CS	PS_MIO1_500	D23
QSPI0_D0	PS_MIO2_500	F23
QSPI0_D1	PS_MIO3_500	C23
QSPI0_D2	PS_MIO4_500	E23
QSPI0_D3	PS_MIO5_500	C24
QSPI1_SCK	PS_MIO9_500	A24
QSPI1_CS	PS_MIO9_500	F24
QSPI1_D0	PS_MIO10_500	E22
QSPI1_D1	PS_MIO11_500	A23
QSPI1_D2	PS_MIO12_500	E21
QSPI1_D3	PS_MIO13_500	F22

Part 5：eMMC Flash

The AX7450 FPGA development board is equipped with a large-capacity 8GB eMMC FLASH chip, model THGBMFG6C1LBAIL, which supports the JEDEC e-MMC V5.0 standard HS-MMC interface with level support of 1.8V or 3.3V. The data width of the eMMC FLASH and ZYNQ connections is 4 bits. Due to the large capacity and non-volatile nature of eMMC FLASH, it can be used as a large-capacity storage device for the ZYNQ system, such as ARM applications, system files and other user data files. The specific models and related parameters of eMMC FLASH are shown in Table 5-1.

Position	Model	Capacity	Factory
U11	THGBMFG6C1LBAIL	8G Byte	TOSHIBA

Table 5-1: eMMC FLASH Specification

eMMC FLASH is connected to the GPIO port of the BANK501 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the SD interface. Figure 5-1 shows the eMMC Flash in the schematic.

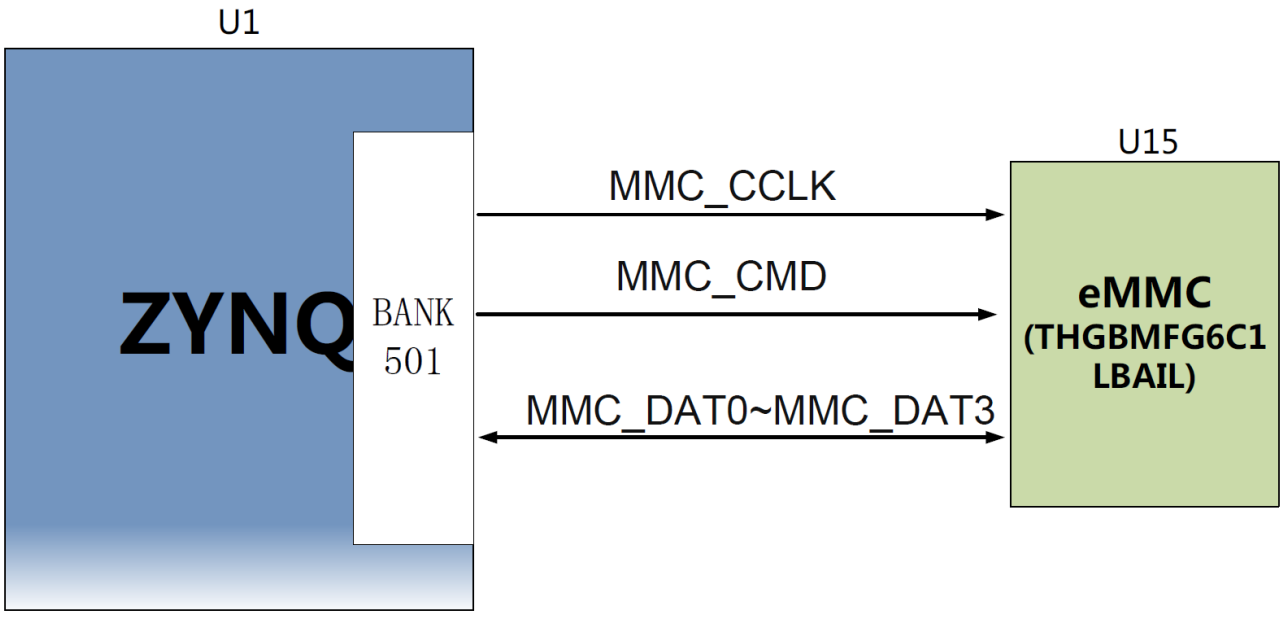


Figure 5-1: eMMC Flash in the Schematic

Pin Assignment of eMMC Flash

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
MMC_CCLK	PS_MIO48_501	C19
MMC_CMD	PS_MIO47_501	A18
MMC_D0	PS_MIO46_501	F20
MMC_D1	PS_MIO49_501	D18
MMC_D2	PS_MIO50_501	A19
MMC_D3	PS_MIO51_501	F19

Part 6: Clock Configuration

The AX7450 FPGA development board provides a single-ended active clock for the PS system and the PL logic, allowing the PS system and PL logic to work independently. In addition, there is a programmable clock chip SI5338P on the board to provide a differential clock source for the high-speed transceiver GTX.

PS system clock source

The ZYNQ chip provides a 33.333MHz clock input to the PS section via the X4 crystal on the FPGA development board. The input of the clock is connected to the pin of the PS_CLK_500 of the BANK500 of the ZYNQ chip. The schematic diagram is shown in Figure 6-1:

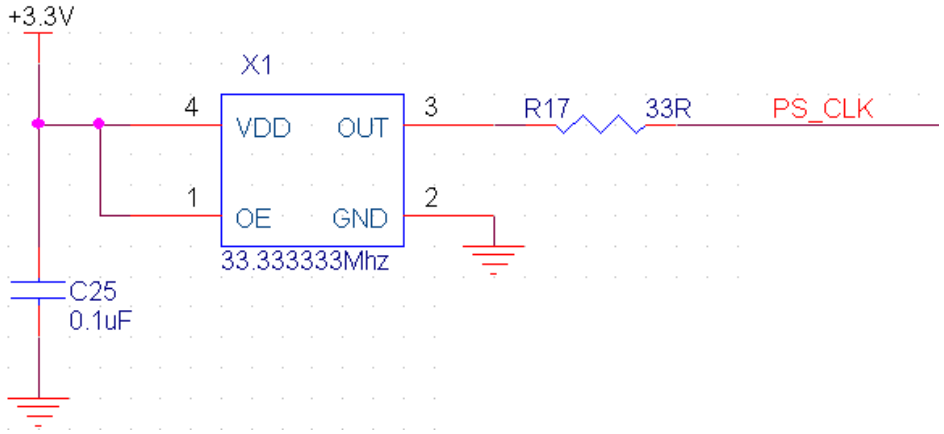


Figure 6-1: Active crystal oscillator to the PS section

PS Clock Pin Assignment

Signal Name	ZYNQ Pin
PS_CLK	A22

PL system clock source

The AX7450 FPGA development board provides a single-ended 50MHz PL system clock source with 1.8V supply. The crystal output is connected to the local clock (SRCC) of the FPGA BANK9, which can be used to drive user

logic circuit within the FPGA. The schematic diagram of the clock source is shown in Figure 6-3.

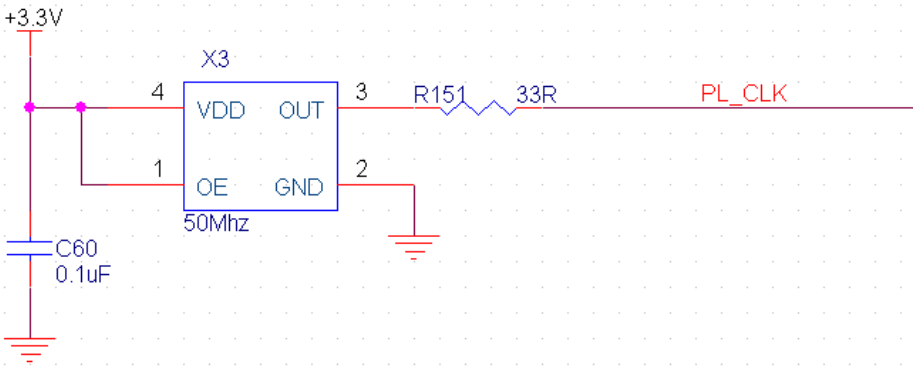


Figure 6-2: PL system clock source

PL Clock pin assignment:

Signal Name	ZYNQ Pin
PL_CLK	AB19

Programmable clock source

The programmable clock source mainly provides reference clocks for the high-speed transceiver GTX and PL DDR controllers. Different data communication of GTX requires different reference clocks. For example, when SFP data communication, it is necessary to provide FPGA with GTX transceiver 125Mhz reference clock. The programmable clock source is implemented by SILICON LABS chip Si5338. The programmable clock source is implemented by SILICON LABS chip Si5338. The ZYNQ chip can configure the Si5338 chip to generate four reference clock signals through the I2C register configuration. The first clock is provided to BANK34 as a reference clock for the PL DDR controller; the second reference clock is provided to BANK110 as the reference clock of the GTX transceiver; the third reference clock is provided to BANK111 as the reference clock of the GTX transceiver; the fourth reference clock is provided to the BANK 10, as the reference clock of FPGA BANK 10. The schematic diagram of the Si5338 circuit design is shown

below:

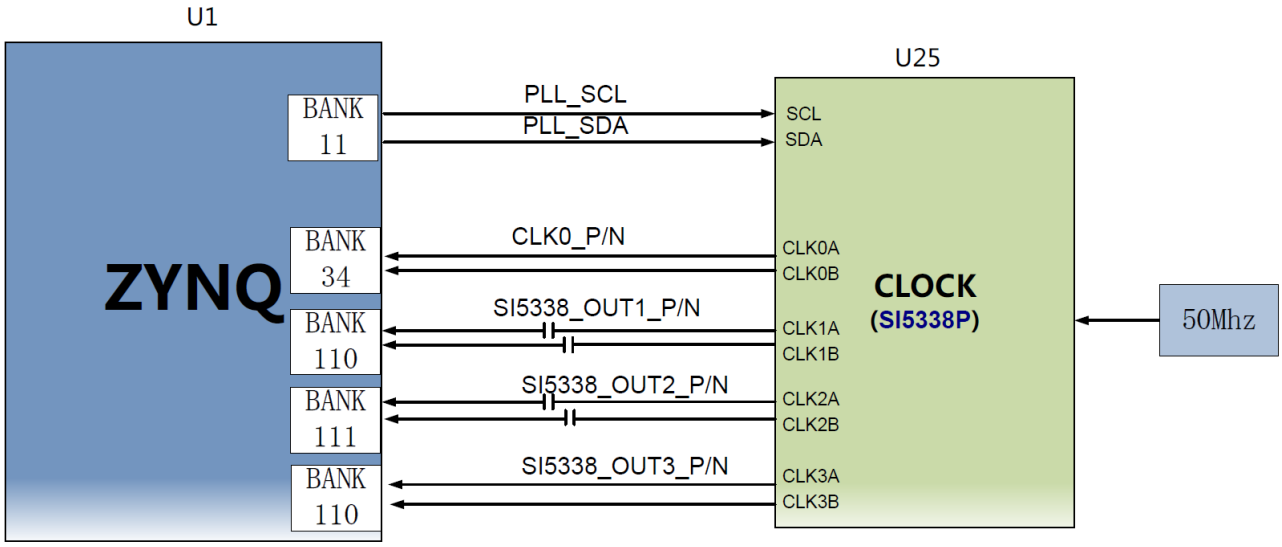


Figure 6-3: Programmable Clock Source

Programmable clock source ZYNQ pin assignment:：

Signal Name	ZYNQ Pin
PLL_SCL	AA22
PLL_SDA	AA23
CLK0_P	F9
CLK0_N	E9
SI5338_OUT1_P	AA9
SI5338_OUT1_N	AA7
SI5338_OUT2_P	W8
SI5338_OUT2_N	W7
SI5338_OUT3_P	AF14
SI5338_OUT3_N	AG14

Part 7: USB to Serial Port

The FPGA development board is equipped with a Uart to USB interface for separate power supply and debugging of the core board. The conversion chip uses the USB-UAR chip of Silicon Labs CP2102GM. The USB interface uses the MINI USB interface. It can be connected to the USB port of the upper PC with a USB cable for separate power supply and serial data communication of the core board.

The schematic diagram of the USB Uart circuit design is shown in Figure 7-1:

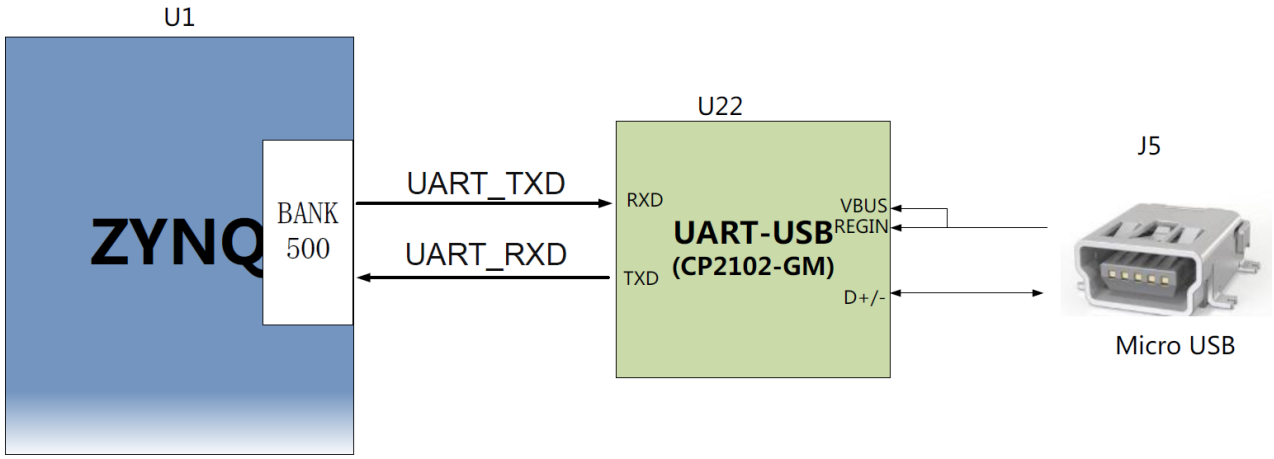


Figure 7-1: USB to serial port schematic

USB to serial port ZYNQ pin assignment:

Signal name	ZYNQ Pin Name	ZYNQ Pin Number	Description
UART_RXD	PS_MIO14_500	B22	Uart data input
UART_TXD	PS_MIO15_500	C22	Uart data output

Part 8: Gigabit Ethernet Interface

The AX7350 FPGA development board has one Gigabit Ethernet interfaces, which is the connected MIO interface of PS system end Bank501. The Ethernet chip uses Micrel's KSZ9031RNX Ethernet PHY chip to provide network communication services to users. The KSZ9031RNX chip supports 10/100/1000 Mbps network transmission rate and communicates with the MAC layer of the Zynq7000 system through the RGMII interface. KSZ9031RNX supports MDI/MDX adaptation, various speed adaptation, Master/Slave adaptation, and supports MDIO bus for PHY register management.

The KSZ9031RNX power-on will detect the level status of some specific IOs to determine their working mode. Table 8-1 describes the default setup information after the GPHY chip is powered up.。

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address is 011
CLK125_EN	Enable 125Mhz clock output selection	Enable
LED_MODE	LED light mode configuration	Single LED light mode
MODE0~MODE3	Link adaptation and full duplex configuration	10/100/1000 adaptive, compatible with full-duplex, half-duplex

Table 8-1: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of ZYNQ and PHY chip KSZ9031RNX is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising edge and falling samples of the clock.

When the network is connected to 100M Ethernet, the data transmission of ZYNQ and PHY chip KSZ9031RNX is communicated through RMII bus, and the transmission clock is 25Mhz. Data is sampled on the rising edge and falling samples of the clock.

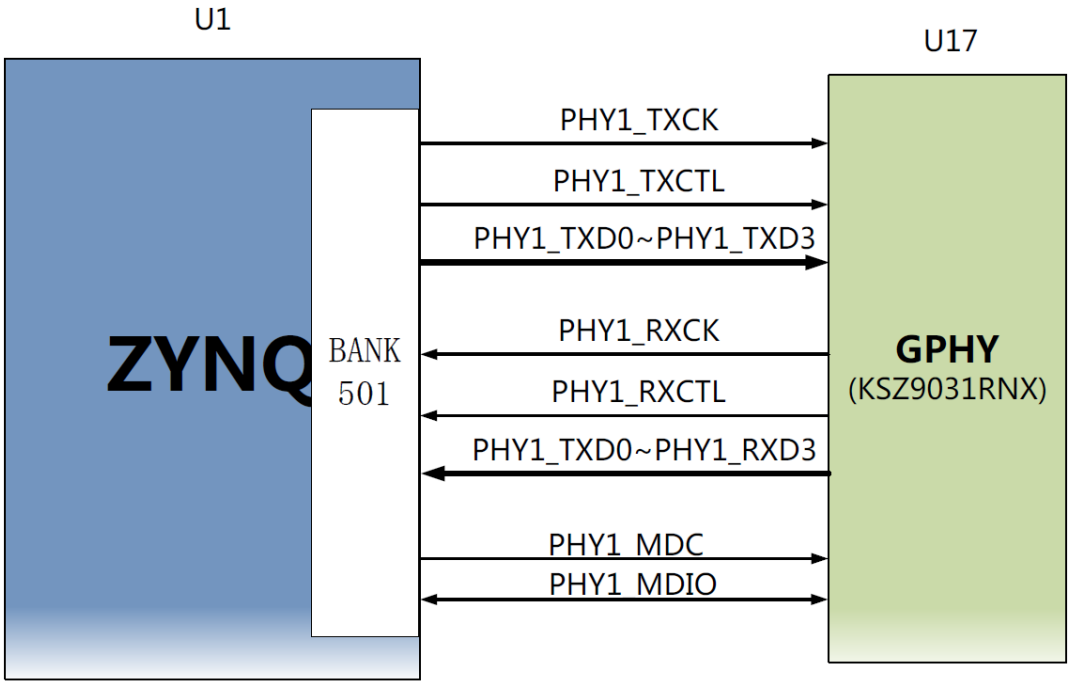


Figure 8-1 detailed the connection of the ZYNQ PS end and GPHY chip

PS side Gigabit Ethernet pin assignments are as follows：

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PHY1_TXCK	PS_MIO16_501	L19	RGMII Transmit Clock
PHY1_TXD0	PS_MIO17_501	K21	Transmit data bit0
PHY1_TXD1	PS_MIO18_501	K20	Transmit data bit1
PHY1_TXD2	PS_MIO19_501	J20	Transmit data bit2
PHY1_TXD3	PS_MIO20_501	M20	Transmit data bit3
PHY1_TXCTL	PS_MIO21_501	J19	Transmit enable signal
PHY1_RXCK	PS_MIO22_501	L20	RGMII Receive Clock
PHY1_RXD0	PS_MIO23_501	J21	Receive data Bit0
PHY1_RXD1	PS_MIO24_501	M19	Receive data Bit1
PHY1_RXD2	PS_MIO25_501	G19	Receive data Bit2
PHY1_RXD3	PS_MIO26_501	M17	Receive data Bit3
PHY1_RXCTL	PS_MIO27_501	G20	Receive data valid signal
PHY1_MDC	PS_MIO52_501	D19	MDIO Management clock
PHY1_MDIO	PS_MIO53_501	C18	MDIO Management data

Part 9: USB2.0 Host Interface

There is one USB2.0 OTG interface on the AX7450 FPGA development board. The USB2.0 transceiver uses a 1.8V, high-speed USB3320C-EZK chip that supports the ULPI standard interface, for high-speed USB2.0 Host mode data communication.

The USB3320C's USB data and control signals are connected to the IO port of the BANK501 on the PS side of the ZYNQ chip. One 24MHz crystals provide clocks for the USB3320C. The USB interface is Mini USB.

The schematic diagram of the ZYNQ processor, USB3320C-EZK chip, shown as Figure 9-1

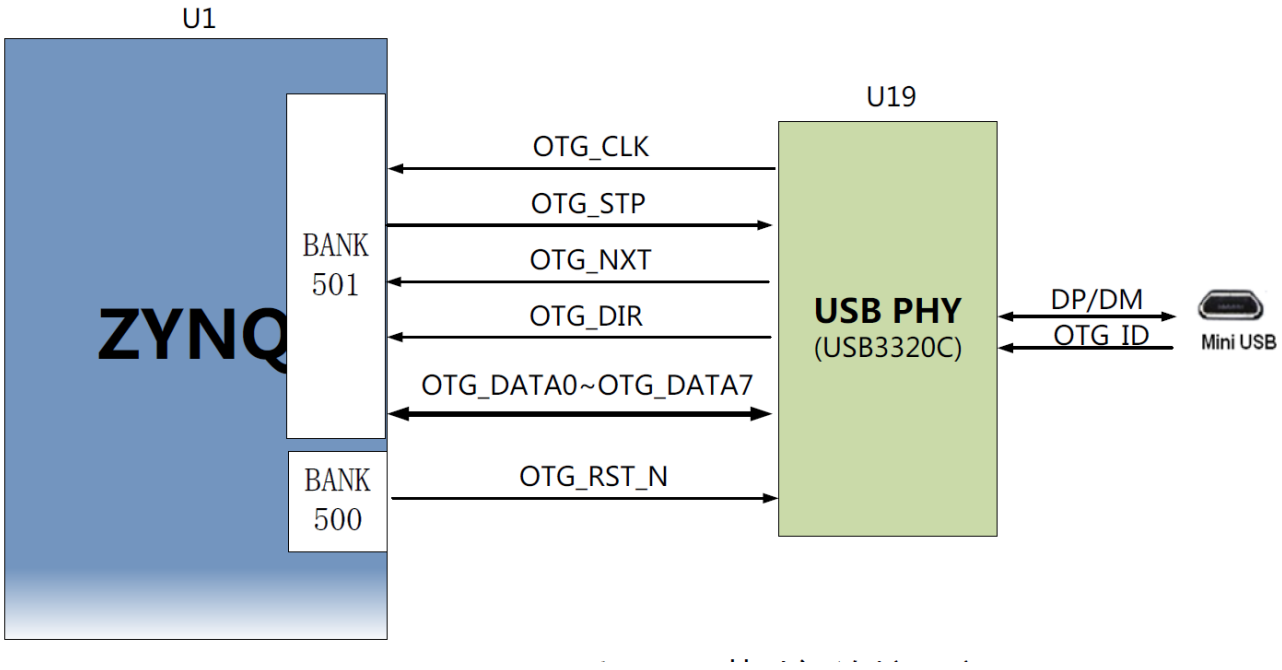


Figure 9-1: The connection between Zynq7000 and USB chip

USB2.0 Pin Assignment：

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
OTG_DATA4	PS_MIO28_501	L17	USB Data Bit4
OTG_DIR	PS_MIO29_501	H22	USB Data Direction Signal

OTG_STP	PS_MIO30_501	L18	USB Stop Signal
OTG_NXT	PS_MIO31_501	H21	USB Next Data Signal
OTG_DATA0	PS_MIO32_501	K17	USB Data Bit0
OTG_DATA1	PS_MIO33_501	G22	USB Data Bit1
OTG_DATA2	PS_MIO34_501	K18	USB Data Bit2
OTG_DATA3	PS_MIO35_501	G21	USB Data Bit3
OTG_CLK	PS_MIO36_501	H17	USB Clock Signal
OTG_DATA5	PS_MIO37_501	B21	USB Data Bit5
OTG_DATA6	PS_MIO38_501	A20	USB Data Bit6
OTG_DATA7	PS_MIO39_501	F18	USB Data Bit7
OTG_RESETN	PS_MIO7_500	A24	USB Reset Signal

Part 10: PCIe Slot

There is a PCIe x8 interface on the AX7450 FPGA development board, and 8 pairs of transceivers are connected to the PCIEx8, which can realize data communication of PCIEex8, PCIEex4, PCIex2, PCIex1.

The transceiver signals of the PCIe interface are directly connected to the GTX transceivers of ZYNQ BANK111 and BANK112. The 8 TX signals and RX signals are connected to the ZYNQ transceiver by differential signals, and the single-channel communication rate can be as high as 5G bit bandwidth.

The PCIe interface schematic of the AX7450 FPGA development board is shown Figure 10-1, in which the TX signal is connected in AC coupling mode.

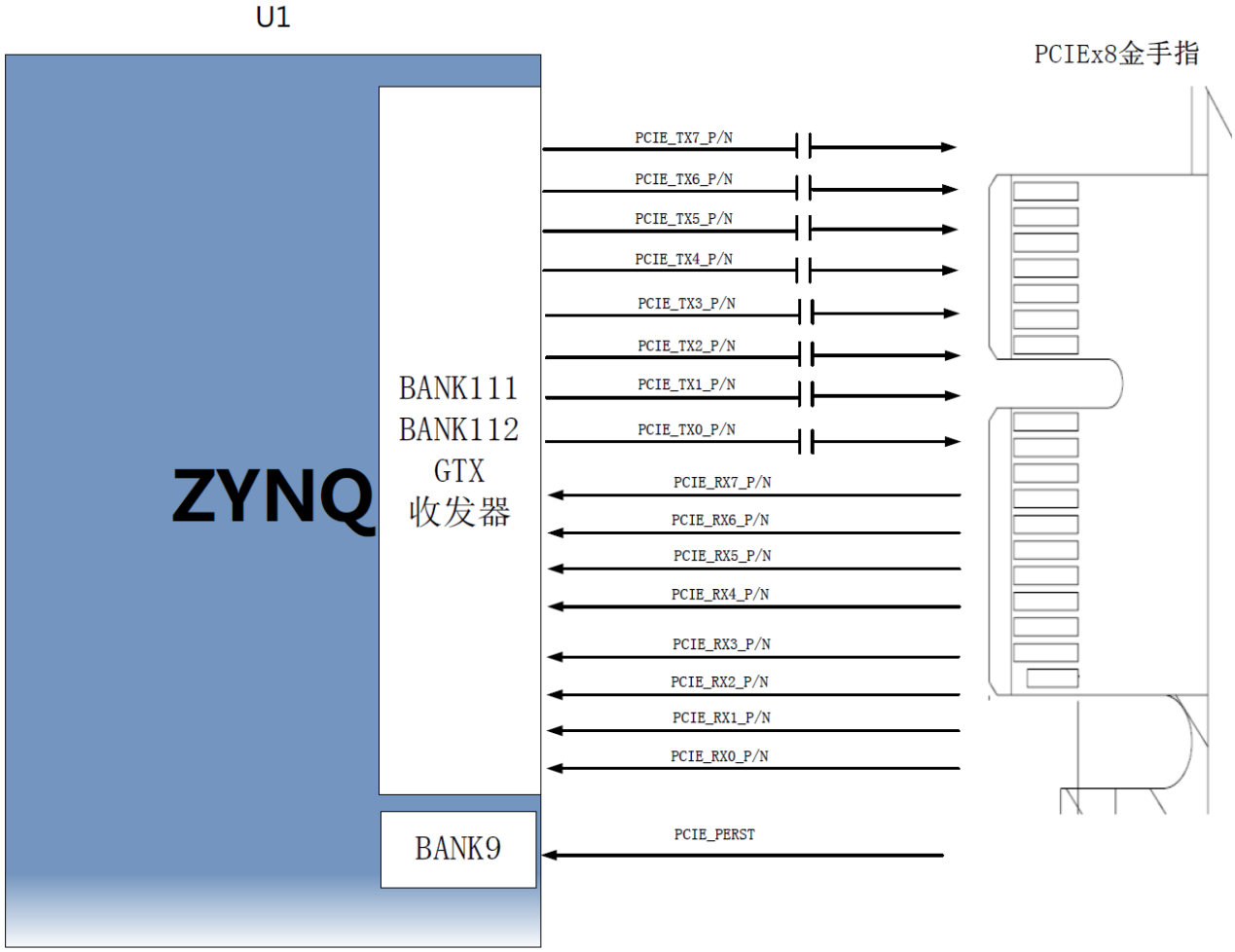


Figure 10-1: PCIe Schematic

The PCIe x8 interface FPGA pin assignment is as follows:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PCIE_RX0_P	BANK112_RX3_P	P6	PCIE channel 0 data receiving positive
PCIE_RX0_N	BANK112_RX3_N	P5	PCIE channel 0 data receiving negative
PCIE_RX1_P	BANK112_RX2_P	T6	PCIE channel 1 data receiving positive
PCIE_RX1_N	BANK112_RX2_N	T5	PCIE channel 1 data receiving negative
PCIE_RX2_P	BANK112_RX1_P	U4	PCIE channel 2 data receiving positive
PCIE_RX2_N	BANK112_RX1_N	U3	PCIE channel 2 data receiving negative
PCIE_RX3_P	BANK112_RX0_P	V6	PCIE channel 3 data receiving positive
PCIE_RX3_N	BANK112_RX0_N	V5	PCIE channel 3 data receiving negative
PCIE_RX4_P	BANK111_RX3_P	AA4	PCIE channel 4 data receiving positive
PCIE_RX4_N	BANK111_RX3_N	AA3	PCIE channel 4 data receiving negative
PCIE_RX5_P	BANK111_RX2_P	Y6	PCIE channel 5 data receiving positive
PCIE_RX5_N	BANK111_RX2_N	Y5	PCIE channel 5 data receiving negative
PCIE_RX6_P	BANK111_RX1_P	AB6	PCIE channel 6 data receiving positive
PCIE_RX6_N	BANK111_RX1_N	AB5	PCIE channel 6 data receiving negative
PCIE_RX7_P	BANK111_RX0_P	AC4	PCIE channel 7 data receiving positive
PCIE_RX7_N	BANK111_RX0_N	AC3	PCIE channel 7 data receiving negative
PCIE_TX0_P	BANK112_TX3_P	N4	PCIE channel 0 data receiving positive
PCIE_TX0_N	BANK112_TX3_N	N3	PCIE channel 0 data receiving negative
PCIE_TX1_P	BANK112_TX2_P	P2	PCIE channel 1 data receiving positive
PCIE_TX1_N	BANK112_TX2_N	P1	PCIE channel 1 data receiving negative
PCIE_TX2_P	BANK112_TX1_P	R4	PCIE channel 2 data receiving positive
PCIE_TX2_N	BANK112_TX1_N	R3	PCIE channel 2 data receiving negative
PCIE_TX3_P	BANK112_TX0_P	T2	PCIE channel 3 data receiving positive
PCIE_TX3_N	BANK112_TX0_N	T1	PCIE channel 3 data receiving negative
PCIE_TX4_P	BANK111_TX3_P	V2	PCIE channel 4 data receiving positive
PCIE_TX4_N	BANK111_TX3_N	V1	PCIE channel 4 data receiving negative
PCIE_TX5_P	BANK111_TX2_P	W4	PCIE channel 5 data receiving positive
PCIE_TX5_N	BANK111_TX2_N	W3	PCIE channel 5 data receiving negative
PCIE_TX6_P	BANK111_TX1_P	Y2	PCIE channel 6 data receiving positive

PCIE_TX6_N	BANK111_TX1_N	Y1	PCIE channel 6 data receiving negative
PCIE_TX7_P	BANK111_TX0_P	AB2	PCIE channel 7 data receiving positive
PCIE_TX7_N	BANK111_TX0_N	AB1	PCIE channel 7 data receiving negative
PCIE_PERST	IO_L12N_T1_MRCC_9	AD19	The reset signal of the PCIE board

Part 11: SD Card Slot

The AX7450 FPGA Development Board contains a Micro SD card interface to provide user access to the SD card memory, the BOOT program for the ZYNQ chip, the Linux operating system kernel, the file system and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of ZYNQ. Since the VCCMIO of the BANK is set to 1.8V, but the data level of the SD card is 3.3V, connected through the TXS02612 level shifter. The schematic of the Zynq7000 PS and SD card connector is shown in Figure 13-1:

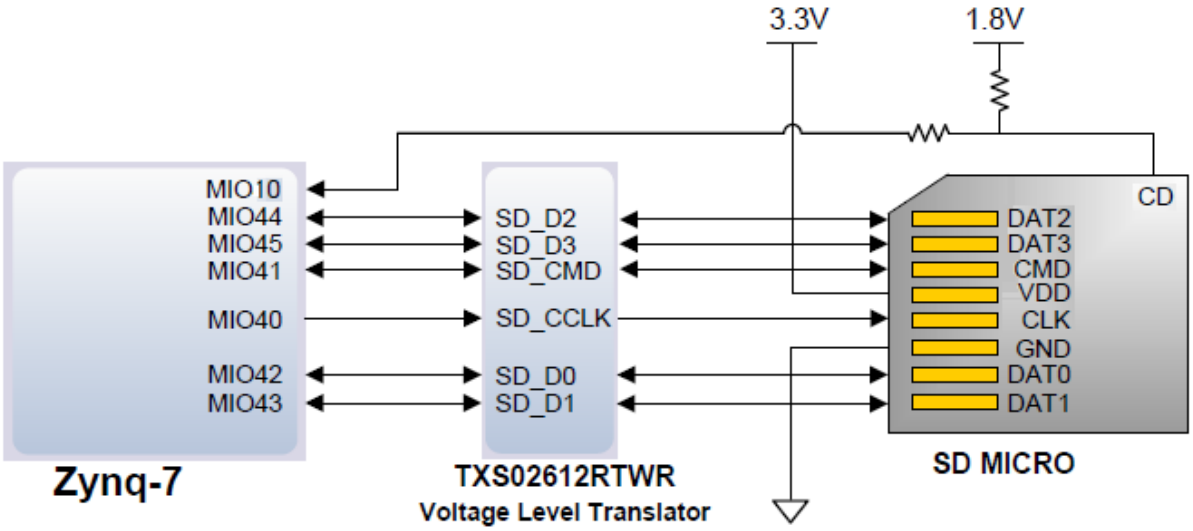


Figure 11-1: SD Card Connection Diagram

SD card slot pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
SD_CLK	PS_MIO40	B20	SD Clock Signal
SD_CMD	PS_MIO41	J18	SD Command Signal
SD_D0	PS_MIO42	D20	SD Data0
SD_D1	PS_MIO43	E18	SD Data1
SD_D2	PS_MIO44	E20	SD Data2
SD_D3	PS_MIO45	H18	SD Data3

Part 12: FMC Connector

The AX7450 FPGA development board has a standard FMC HPC expansion port that can be connected to various FMC modules of XILINX or ALINX (HDMI input and output modules, binocular camera modules, high-speed AD modules, etc.). The FMC expansion port contains 84 pairs of differential IO signals and one high-speed GTX transceiver signal.

The 84 pairs of differential signals of the FMC expansion port are connected to the IO of BANK10~13 of the ZYNQ chip. The IO level standard is determined by the voltage VADJ and VIO_B of the BANK. These two power supplies can be configured to change the output voltage of the PMIC chip LP873220 through the program. For example, the voltage of VADJ and VIO_B is 2.5V, so that 84 pairs of differential signals support LVDS data communication. The other 8 GTX transceiver signals and reference clock signals are respectively connected to the GTX transceiver and clock input of ZYNQ BANK109 and BANK110

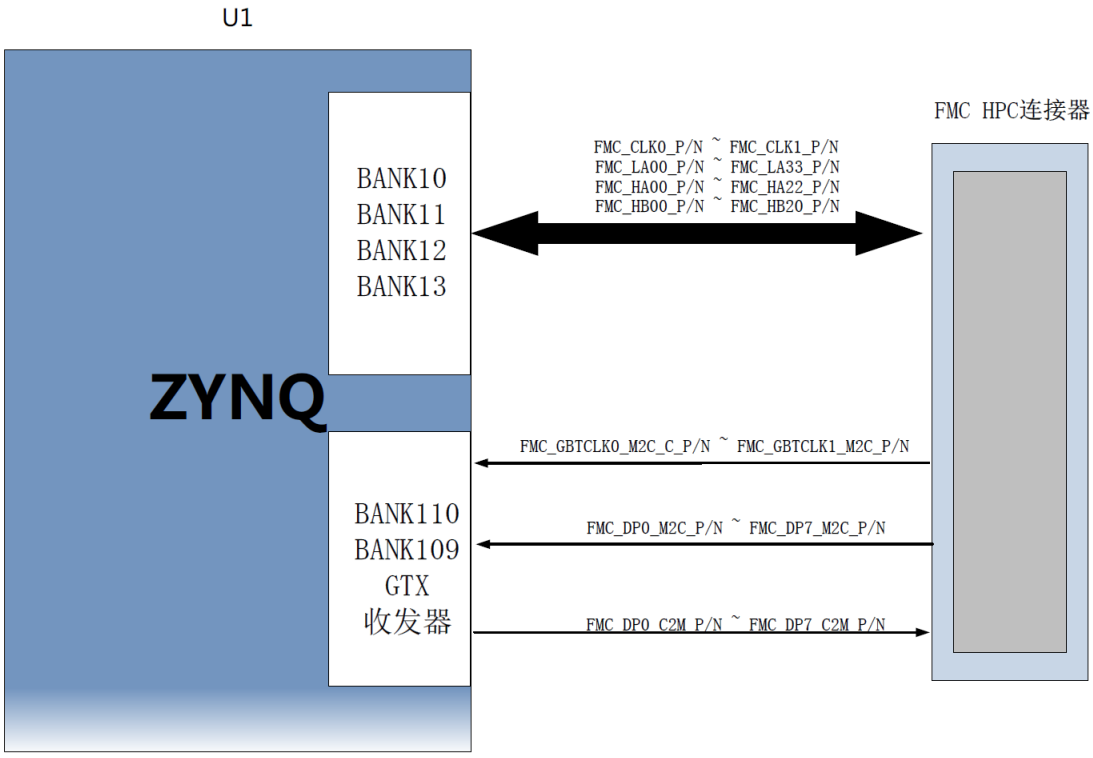


Figure 12-1: FMC connection diagram

FMC connector pin assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
J2	FMC_CLK1_C2M_P	R25	FMC 1st Channel output reference clock P
J3	FMC_CLK1_C2M_N	R26	FMC 1st Channel output reference clock N
H4	FMC_CLK0_M2C_P	AE13	FMC 0th Channel input reference clock P
H5	FMC_CLK0_M2C_N	AF13	FMC 0th Channel input reference clock N
G2	FMC_CLK0_ C2M _P	AF20	FMC 0st Channel input reference clock P
G3	FMC_CLK0_ C2M _N	AG20	FMC 0st Channel input reference clock N
G6	FMC_LA00_CC_P	AF15	FMC LA 0th Channel data (clock) P
G7	FMC_LA00_CC_N	AG15	FMC LA 0th Channel data (clock) N
D8	FMC_LA01_CC_P	AG17	FMC LA 1st Channel data (clock) P
D9	FMC_LA01_CC_N	AG16	FMC LA 1st Channel data (clock)N
H7	FMC_LA02_P	AA15	FMC LA 2nd Channel data P
H8	FMC_LA02_N	AA14	FMC LA 2nd Channel data N
G9	FMC_LA03_P	AC14	FMC LA 3rd Channel data P
G10	FMC_LA03_N	AC13	FMC LA 3rd Channel data N
H10	FMC_LA04_P	AD14	FMC LA 4th Channel data P
H11	FMC_LA04_N	AD13	FMC LA 4thChannel data N
D11	FMC_LA05_P	AG12	FMC LA 5th Channel data P
D12	FMC_LA05_N	AH12	FMC LA 5thChannel data N
C10	FMC_LA06_P	AD16	FMC LA 6th Channel data P
C11	FMC_LA06_N	AD15	FMC LA 6thChannel data N
H13	FMC_LA07_P	AH14	FMC LA 7th Channel data P
H14	FMC_LA07_N	AH13	FMC LA 7thChannel data N
G12	FMC_LA08_P	AE12	FMC LA 8th Channel data P
G13	FMC_LA08_N	AF12	FMC LA 8thChannel data N
D14	FMC_LA09_P	AJ14	FMC LA 9th Channel data P
D15	FMC_LA09_N	AJ13	FMC LA 9thChannel data N
C14	FMC_LA10_P	AJ15	FMC LA 10th Channel data P
C15	FMC_LA10_N	AK15	FMC LA 10thChannel data N
H16	FMC_LA11_P	AJ16	FMC LA 11th Channel data P
H17	FMC_LA11_N	AK16	FMC LA 11thChannel data N

G15	FMC_LA12_P	AE16	FMC LA 12th Channel data P
G16	FMC_LA12_N	AE15	FMC LA 12thChannel data N
D17	FMC_LA13_P	AH17	FMC LA 13th Channel data P
D18	FMC_LA13_N	AH16	FMC LA 13thChannel data N
C18	FMC_LA14_P	AF18	FMC LA 14th Channel data P
C19	FMC_LA14_N	AF17	FMC LA 14thChannel data N
H19	FMC_LA15_P	AE18	FMC LA 15th Channel data P
H20	FMC_LA15_N	AE17	FMC LA 15thChannel data N
G18	FMC_LA16_P	AH18	FMC LA 16th Channel data P
G19	FMC_LA16_N	AJ18	FMC LA 16thChannel data N
D20	FMC_LA17_CC_P	AG21	FMC LA 17th Channel data (clock) P
D21	FMC_LA17_CC_N	AH21	FMC LA 17th Channel data (clock)N
C22	FMC_LA18_CC_P	AD23	FMC LA 18th Channel data (clock) P
C23	FMC_LA18_CC_N	AE23	FMC LA 18th Channel data (clock)N
H22	FMC_LA19_P	AB21	FMC LA 19th Channel data P
H23	FMC_LA19_N	AB22	FMC LA 19thChannel data N
G21	FMC_LA20_P	W21	FMC LA 20th Channel data P
G22	FMC_LA20_N	Y21	FMC LA 20thChannel data N
H25	FMC_LA21_P	AK17	FMC LA 21th Channel data P
H26	FMC_LA21_N	AK18	FMC LA 21thChannel data N
G24	FMC_LA22_P	AD21	FMC LA 22th Channel data P
G25	FMC_LA22_N	AE21	FMC LA 22thChannel data N
D23	FMC_LA23_P	AF19	FMC LA 23th Channel data P
D24	FMC_LA23_N	AG19	FMC LA 23thChannel data N
H28	FMC_LA24_P	AG22	FMC LA 24th Channel data P
H29	FMC_LA24_N	AH22	FMC LA 24thChannel data N
G27	FMC_LA25_P	AJ21	FMC LA 25th Channel data P
G28	FMC_LA25_N	AK21	FMC LA 25thChannel data N
D26	FMC_LA26_P	AH19	FMC LA 26th Channel data P
D27	FMC_LA26_N	AJ19	FMC LA 26thChannel data N
C26	FMC_LA27_P	AJ20	FMC LA 27th Channel data P
C27	FMC_LA27_N	AK20	FMC LA 27thChannel data N
H31	FMC_LA28_P	AJ23	FMC LA 28th Channel data P

H32	FMC_LA28_N	AJ24	FMC LA 28thChannel data N
G30	FMC_LA29_P	AK22	FMC LA 29th Channel data P
G31	FMC_LA29_N	AK23	FMC LA 29thChannel data N
H34	FMC_LA30_P	AG24	FMC LA 30th Channel data P
H35	FMC_LA30_N	AG25	FMC LA 30thChannel data N
G33	FMC_LA31_P	AH23	FMC LA 31th Channel data P
G34	FMC_LA31_N	AH24	FMC LA 31thChannel data N
H37	FMC_LA32_P	AC24	FMC LA 32th Channel data P
H38	FMC_LA32_N	AD24	FMC LA 32thChannel data N
G36	FMC_LA33_P	AF23	FMC LA 33th Channel data P
G37	FMC_LA33_N	AF24	FMC LA 33thChannel data N
F4	FMC_HA00_CC_P	AC28	FMC HA 0th Channel data (clock) P
F5	FMC_HA00_CC_N	AD28	FMC HA 0th Channel data (clock) N
E2	FMC_HA01_CC_P	AB27	FMC HA 1st Channel data (clock) P
E3	FMC_HA01_CC_N	AC27	FMC HA 1st Channel data (clock)N
K7	FMC_HA02_P	AJ26	FMC HA 2nd Channel data P
K8	FMC_HA02_N	AK26	FMC HA 2nd Channel data N
J6	FMC_HA03_P	AE25	FMC HA 3rd Channel data P
J7	FMC_HA03_N	AF25	FMC HA 3rd Channel data N
F7	FMC_HA04_P	AB25	FMC HA 4th Channel data P
F8	FMC_HA04_N	AB26	FMC HA 4thChannel data N
E6	FMC_HA05_P	Y26	FMC HA 5th Channel data P
E7	FMC_HA05_N	Y27	FMC HA 5thChannel data N
K10	FMC_HA06_P	Y28	FMC HA 6th Channel data P
K11	FMC_HA06_N	AA29	FMC HA 6thChannel data N
J9	FMC_HA07_P	AJ28	FMC HA 7th Channel data P
J10	FMC_HA07_N	AJ29	FMC HA 7thChannel data N
F10	FMC_HA08_P	AD25	FMC HA 8th Channel data P
F11	FMC_HA08_N	AE26	FMC HA 8thChannel data N
E9	FMC_HA09_P	AC26	FMC HA 9th Channel data P
E10	FMC_HA09_N	AD26	FMC HA 9thChannel data N
K13	FMC_HA10_P	AA27	FMC HA 10th Channel data P
K14	FMC_HA10_N	AA28	FMC HA 10thChannel data N

J12	FMC_HA11_P	Y30	FMC HA 11th Channel data P
J13	FMC_HA11_N	AA30	FMC HA 11thChannel data N
F13	FMC_HA12_P	AG26	FMC HA 12th Channel data P
F14	FMC_HA12_N	AG27	FMC HA 12thChannel data N
F14	FMC_HA12_N	AG27	FMC HA 13th Channel data P
E12	FMC_HA13_P	AE27	FMC HA 13thChannel data N
E13	FMC_HA13_N	AF27	FMC HA 14th Channel data P
J15	FMC_HA14_P	AF29	FMC HA 14thChannel data N
F16	FMC_HA15_P	AK27	FMC HA 15th Channel data P
F17	FMC_HA15_N	AK28	FMC HA 15thChannel data N
E15	FMC_HA16_P	AH26	FMC HA 16th Channel data P
E16	FMC_HA16_N	AH27	FMC HA 16thChannel data N
K16	FMC_HA17_CC_P	AE28	FMC HA 17th Channel data (clock) P
K17	FMC_HA17_CC_N	AF28	FMC HA 17th Channel data (clock)N
J18	FMC_HA18_P	AF30	FMC HA 18th Channel data P
J19	FMC_HA18_N	AG30	FMC HA 18th Channel data N
F19	FMC_HA19_P	AJ30	FMC HA 19th Channel data P
F20	FMC_HA19_N	AK30	FMC HA 19thChannel data N
E18	FMC_HA20_P	AH28	FMC HA 20th Channel data P
E19	FMC_HA20_N	AH29	FMC HA 20thChannel data N
K19	FMC_HA21_P	AB29	FMC HA 21th Channel data P
K20	FMC_HA21_N	AB30	FMC HA 21thChannel data N
J21	FMC_HA22_P	AD30	FMC HA 22th Channel data P
J22	FMC_HA22_N	AE30	FMC HA 22thChannel data N
K22	FMC_HA23_P	AC29	FMC HA 23th Channel data P
K23	FMC_HA23_N	AD29	FMC HA 23thChannel data N
K25	FMC_HB00_CC_P	U25	FMC HB 0th Channel data (clock) P
K26	FMC_HB00_CC_N	V26	FMC HB 0th Channel data (clock) N
J24	FMC_HB01_P	P21	FMC HB 1st Channel data P
J25	FMC_HB01_N	R21	FMC HB1st Channel data N
F22	FMC_HB02_P	U22	FMC HB 2nd Channel data P
F23	FMC_HB02_N	V22	FMC HB 2nd Channel data N
E21	FMC_HB03_P	R22	FMC HB 3rd Channel data P

E22	FMC_HB03_N	R23	FMC HB 3rd Channel data N
F25	FMC_HB04_P	W25	FMC HB 4th Channel data P
F26	FMC_HB04_N	W26	FMC HB 4thChannel data N
E24	FMC_HB05_P	U24	FMC HB 5th Channel data P
E25	FMC_HB05_N	V24	FMC HB 5thChannel data N
K28	FMC_HB06_CC_P	U26	FMC HB 6th Channel data P
K29	FMC_HB06_CC_N	U27	FMC HB 6thChannel data N
J27	FMC_HB07_P	T22	FMC HB 7th Channel data P
J28	FMC_HB07_N	T23	FMC HB 7thChannel data N
F28	FMC_HB08_P	V28	FMC HB 8th Channel data P
F29	FMC_HB08_N	V29	FMC HB 8thChannel data N
E27	FMC_HB09_P	V27	FMC HB 9th Channel data P
E28	FMC_HB09_N	W28	FMC HB 9thChannel data N
K31	FMC_HB10_P	W29	FMC HB 10th Channel data P
K32	FMC_HB10_N	W30	FMC HB 10thChannel data N
J30	FMC_HB11_P	T24	FMC HB 11th Channel data P
J31	FMC_HB11_N	T25	FMC HB 11thChannel data N
F31	FMC_HB12_P	T30	FMC HB 12th Channel data P
F32	FMC_HB12_N	U30	FMC HB 12thChannel data N
E30	FMC_HB13_P	T29	FMC HB 13th Channel data P
E31	FMC_HB13_N	U29	FMC HB 13thChannel data N
K34	FMC_HB14_P	N29	FMC HB 14th Channel data P
K35	FMC_HB14_N	P29	FMC HB 14thChannel data N
J33	FMC_HB15_P	R28	FMC HB 15th Channel data P
J34	FMC_HB15_N	T28	FMC HB 15thChannel data N
F34	FMC_HB16_P	P30	FMC HB 16th Channel data P
F35	FMC_HB16_N	R30	FMC HB 16thChannel data N
K37	FMC_HB17_CC_P	R27	FMC HB 17th Channel data (clock) P
K38	FMC_HB17_CC_N	T27	FMC HB 17th Channel data (clock)N
J36	FMC_HB18_P	P23	FMC HB 18th Channel data P
J37	FMC_HB18_N	P24	FMC HB 18th Channel data N
E33	FMC_HB19_P	P25	FMC HB 19th Channel data P
E34	FMC_HB19_N	P26	FMC HB 19thChannel data N

F37	FMC_HB20_P	N26	FMC HB 20th Channel data P
F38	FMC_HB20_N	N27	FMC HB 20thChannel data N
E36	FMC_HB21_P	N28	FMC HB 21th Channel data P
E37	FMC_HB21_N	P28	FMC HB 21thChannel data N
D4	FMC_GBTCLK0_M2C_P	AD10	Transceiver reference clock 0 input P
D5	FMC_GBTCLK0_M2C_N	AD9	Transceiver reference clock 0 input N
B20	FMC_GBTCLK1_M2C_P	AA8	Transceiver reference clock 1 input P
B21	FMC_GBTCLK1_M2C_N	AA7	Transceiver reference clock 1 input N
C6	FMC_DP0_M2C_P	AH10	Transceiver data 0 input P
C7	FMC_DP0_M2C_N	AH9	Transceiver data 0 input N
A2	FMC_DP1_M2C_P	AJ8	Transceiver data 1 input P
A3	FMC_DP1_M2C_N	AJ7	Transceiver data 1 input N
A6	FMC_DP2_M2C_P	AG8	Transceiver data 2 input P
A7	FMC_DP2_M2C_N	AG7	Transceiver data 2 input N
A10	FMC_DP3_M2C_P	AE8	Transceiver data 3 input P
A11	FMC_DP3_M2C_N	AE7	Transceiver data 3 input N
A14	FMC_DP4_M2C_P	AH6	Transceiver data 4 input P
A15	FMC_DP4_M2C_N	AH5	Transceiver data 4 input N
A18	FMC_DP5_M2C_P	AG4	Transceiver data 5 input P
A19	FMC_DP5_M2C_N	AG3	Transceiver data 5 input N
B16	FMC_DP6_M2C_P	AF6	Transceiver data 6 input P
B17	FMC_DP6_M2C_N	AF5	Transceiver data 6 input N
B12	FMC_DP7_M2C_P	AD6	Transceiver data 7 input P
B13	FMC_DP7_M2C_N	AD5	Transceiver data 7 input N
C2	FMC_DP0_C2M_P	AK10	Transceiver data 0 input P
C3	FMC_DP0_C2M_N	AK9	Transceiver data 0 input N
A22	FMC_DP1_C2M_P	AK6	Transceiver data 1 input P
A23	FMC_DP1_C2M_N	AK5	Transceiver data 1 input N
A26	FMC_DP2_C2M_P	AJ4	Transceiver data 2 input P
A27	FMC_DP2_C2M_N	AJ3	Transceiver data 2 input N
A30	FMC_DP3_C2M_P	AK2	Transceiver data 3 input P
A31	FMC_DP3_C2M_N	AK1	Transceiver data 3 input N
A34	FMC_DP4_C2M_P	AH2	Transceiver data 4 input P

A35	FMC_DP4_C2M_N	AH1	Transceiver data 4 input N
A38	FMC_DP5_C2M_P	AF2	Transceiver data 5 input P
A39	FMC_DP5_C2M_N	AF1	Transceiver data 5 input N
B36	FMC_DP6_C2M_P	AE4	Transceiver data 6 input P
B37	FMC_DP6_C2M_N	AE3	Transceiver data 6 input N
B32	FMC_DP7_C2M_P	AD2	Transceiver data 7 input P
B33	FMC_DP7_C2M_N	AD1	Transceiver data 7 input N

Part 13: LED Light

There are 9 single-color LED lights and 1 dual-color LED light on the AX7450 development board. Single-color LED lights include 1 power indicator; 1 DONE configuration indicator; 2 serial communication indicators, and 4 PL control indicators. The two-color LED lights are mounted on the side of the FPGA development board and controlled by PL's IO. Four single-color LED lights are connected to the IO of BANK10, and two-color LED lights are connected to the IO of BANK9.

Figure 13-1 detailed the LED light hardware connection diagram

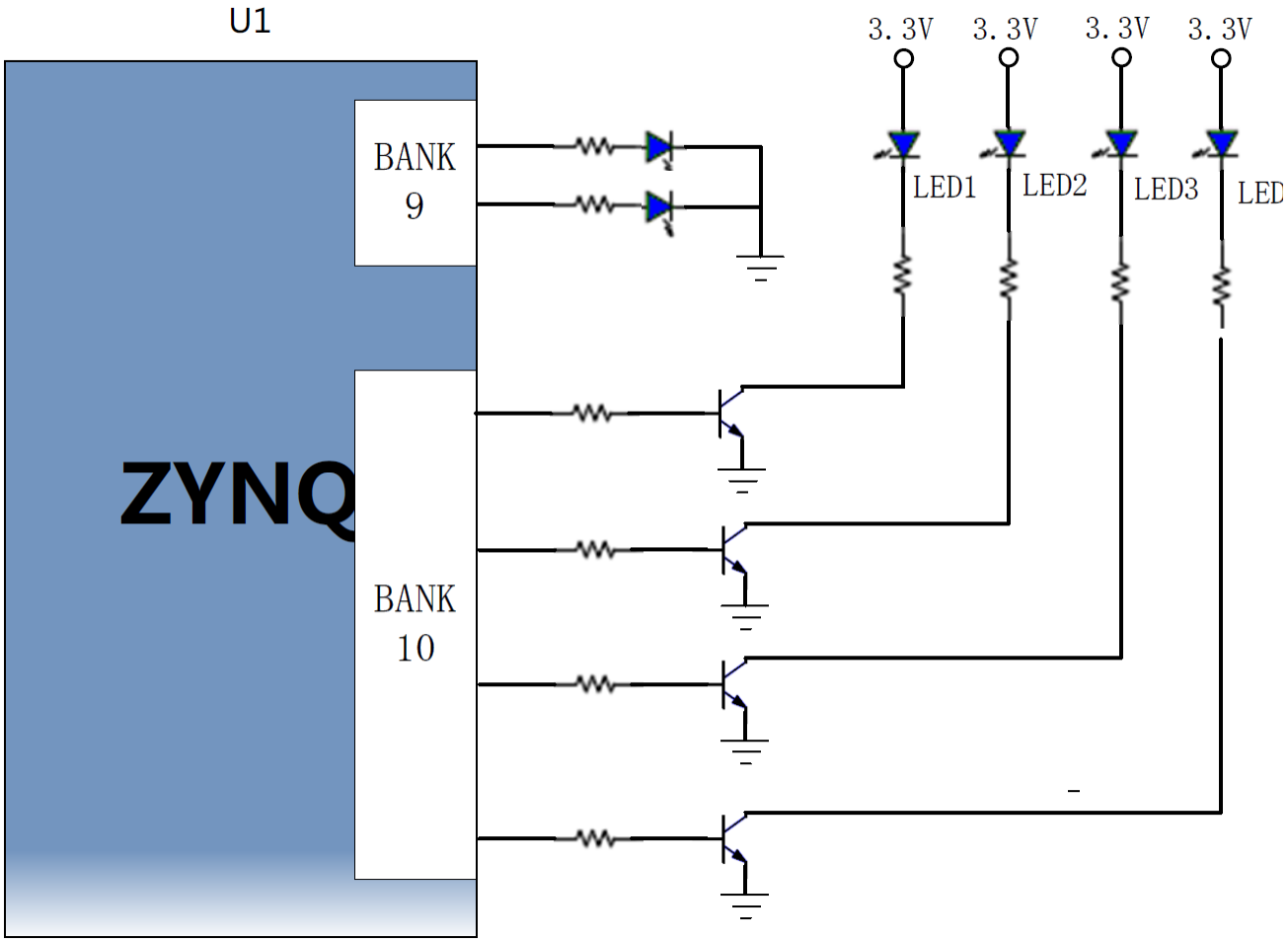


Figure 13-1: The User LEDs Hardware Connection Diagram

Pin assignment of user LED lights

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PL_LED1	IO_L23P_T3_10	AC16	User single-color PL LED1 light
PL_LED2	IO_L23N_T3_10	AB17	User single-color PL LED2 light
PL_LED3	IO_L24P_T3_10	AB16	User single-color PL LED3 light
PL_LED4	IO_L24N_T3_10	AA17	User single-color PL LED4 light
TEST_LED1	IO_L11N_T1_SRCC_9	AC19	User dual-color PL LED1 light
TEST_LED2	IO_L12P_T1_MRCC_9	AD18	User dual-color PL LED2 light

Part 14: Reset Key and User Key

The AX7450 FPGA development board has one reset key RESET and one user key. The reset signal is connected to the PS reset pin of the ZYNQ chip. The user can use this reset key to reset the ZYNQ system. One user key is connected to the IO of the PS. The reset key and the user key are all active low. The connection between the reset key and the user key is shown in Figure 16-1.

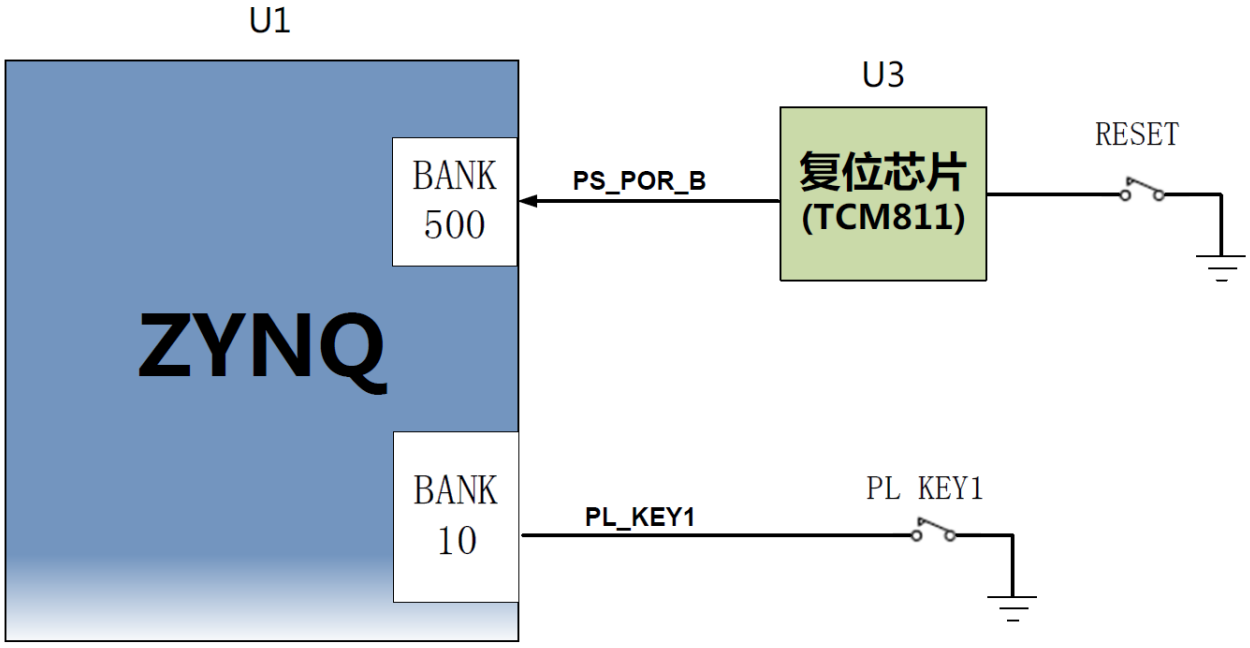


Figure 14-1: Keys Connection Schematic

ZYNQ pin assignment of the button

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_POR_B	PS_POR_B_500	D21	ZYNQ System Reset Signal
PL_KEY1	IO_L21N_T3_DQS_10	AC12	PL Key 1 input

Part15: SMA Interface

There are 2 SMA interfaces on the AX7450 FPGA development board, which are convenient for users to input or output differential clock signals or separate clock signals through SMA lines. The signals of the SMA interface are connected to the IO of BANK9. The default standard level is 3.3V. The SMA schematic is shown in Figure 15-1:

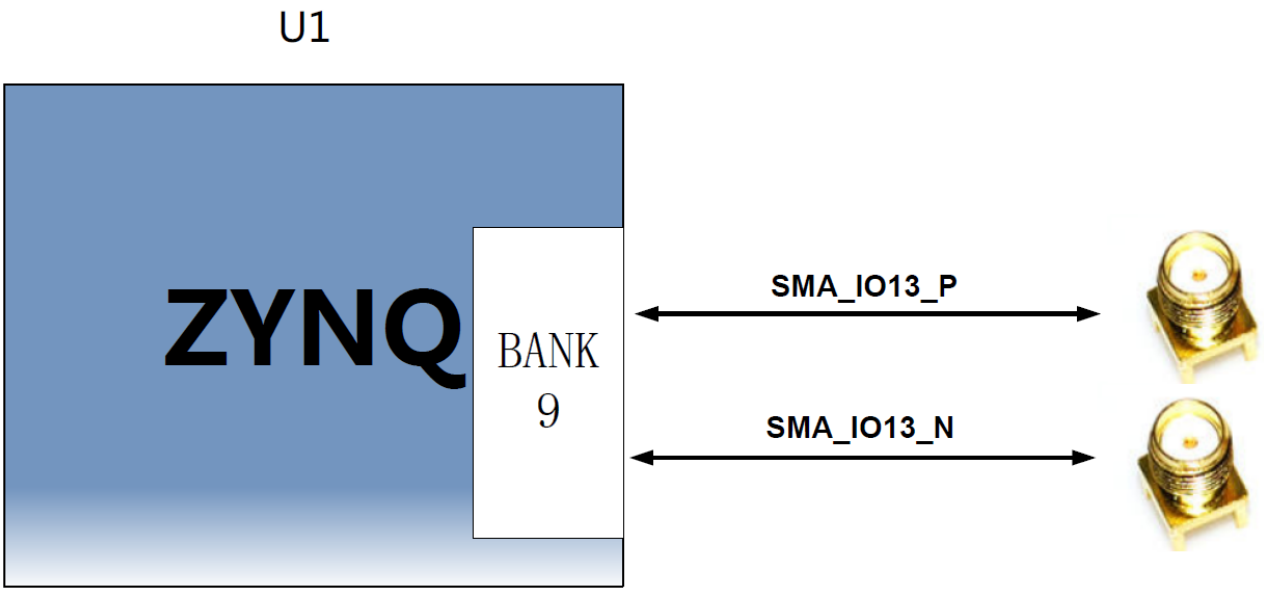


Figure 15-1: SMA Interface Schematic

ZYNQ pin assignment of SMA Interface

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_POR_B	PS_POR_B_500	D21	SMA interface input 1
PL_KEY1	IO_L21N_T3_DQS_10	AC12	SMA interface input 2

Part16: JTAG debug port

The JTAG interface is reserved on the AX7450 FPGA development board for downloading ZYNQ programs or firmware programs to FLASH. In order to avoid damage to the ZYNQ chip caused by hot plugging, a protection diode is added to the JTAG signal to ensure that the signal voltage is within the range accepted by the FPGA and to avoid damage to the ZYNQ chip.

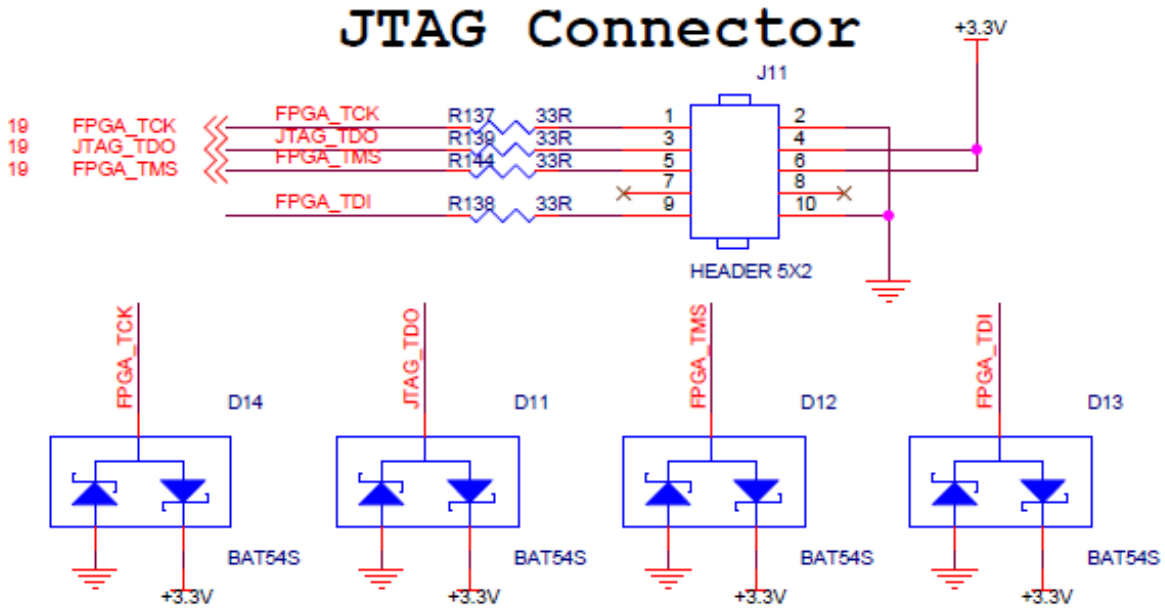


Figure 16-1: JTAG Interface Schematic

On the AX7350 FPGA development board, the JTAG interface is in the form of USB interface. Users can connect the PC and JTAG interface to the ZYNQ system debugging through the USB cable provided by us.

Part 17: DIP Switch Configuration

The AX7450 FPGA development board has a 2-bit DIP switch SW1 to configure the ZYNQ system's start up mode. The AX7450 system development platform supports three boot modes. The three boot modes are JTAG debug mode, QSPI FLASH and SD card boot mode. After the XC7Z100 chip is powered on, it will detect the level of the corresponding MIO port (MIO5 and MIO4) to determine which start up mode. The user can select different start up modes through the DIP switch SW1 on the board. The SW1 start up mode configuration is shown in Table 17-1.

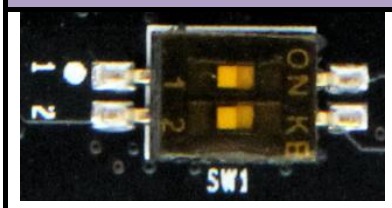
SW1	Switch Position（1，2）	MIO5,MIO4 Level	Start Mode
	ON、ON	0、0	JTAG
	OFF、OFF	1、1	SD Card
	OFF、ON	1、0	QSPI FLASH

Table 17-1: SW1 start mode configuration

Part 18: Power Supply

The power input voltage of the development board is DC12V, and the external +12V power supply supplies power to the board. The +12V input power supply generates +1.0V ZYNQ core power through the DCDC power chip MYMGK1R820ERSR. In addition, +12V generates +5V and 1.5V power through the DC/DC power chip TPS54620, and the +5V power generates +3.3V and +1.8V five-way power through the DCDC chip TPS54620 and TLV62130. The VADJ and VIO_B of the FMC interface are generated by a PMIC power chip output, and these two power sources can be configured by software.The schematic diagram of the power supply design on the AX7450 FPGA development board is shown in Figure 18-1

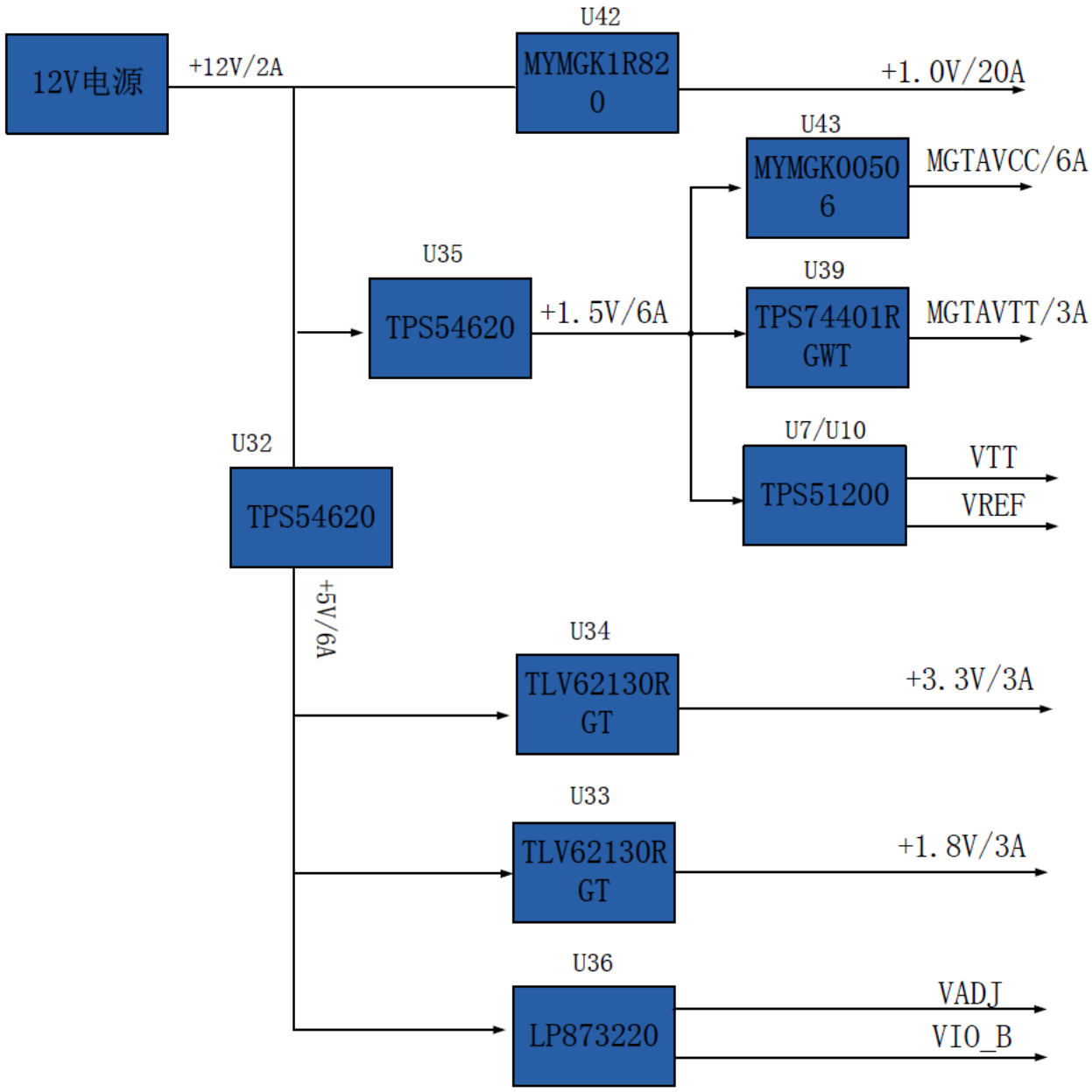


Figure 18-1: Power interface section in the schematic

The functions of each power distribution are shown in the following table:：

Power Supply	Function
+1.0V	ZYNQ PS and PL section Core Voltage
+1.8V	ZYNQ PS and PL partial auxiliary voltage,BANK501 IO Voltage，eMMC，HDMI
+3.3V	ZYNQ Bank0,Bank500，QSIP FLASH, Clock Crystal, SD Card，SFP optical module
+1.5V	DDR3, ZYNQ Bank501, Bank33,Bank34,Bank35

VADJ	ZYNQ Bank10, Bank11,Bank12, FMC
VREF, VTT（+0.75V）	PS DDR3，PL DDR3
MGTAVCC(+1.0V)	ZYNQ Bank109,Bank110, Bank111,Bank112
MGTAVTT(+1.2V)	ZYNQ Bank109,Bank110, Bank111,Bank112

Because the power supply of the ZYNQ FPGA has the power-on sequence requirements, in the circuit design, we have designed according to the power requirements of the chip. The power-on sequence is +1.0V->+1.8V->(+1.5 V, +3.3V, VCCIO) circuit design to ensure the normal operation of the chip.

Part 19: Fan

Because ZYNQ7100 generates a lot of heat when it works normally, we add a heat sink and fan to the chip on the board to prevent the chip from overheating. The control of the fan is controlled by the ZYNQ chip. The control pin is connected to the IO of the BANK11. If the IO level output is low, the MOSFET is turned on and the fan is working. If the IO level output is high, the fan stops. The fan design on the board is shown in Figure 19-1.

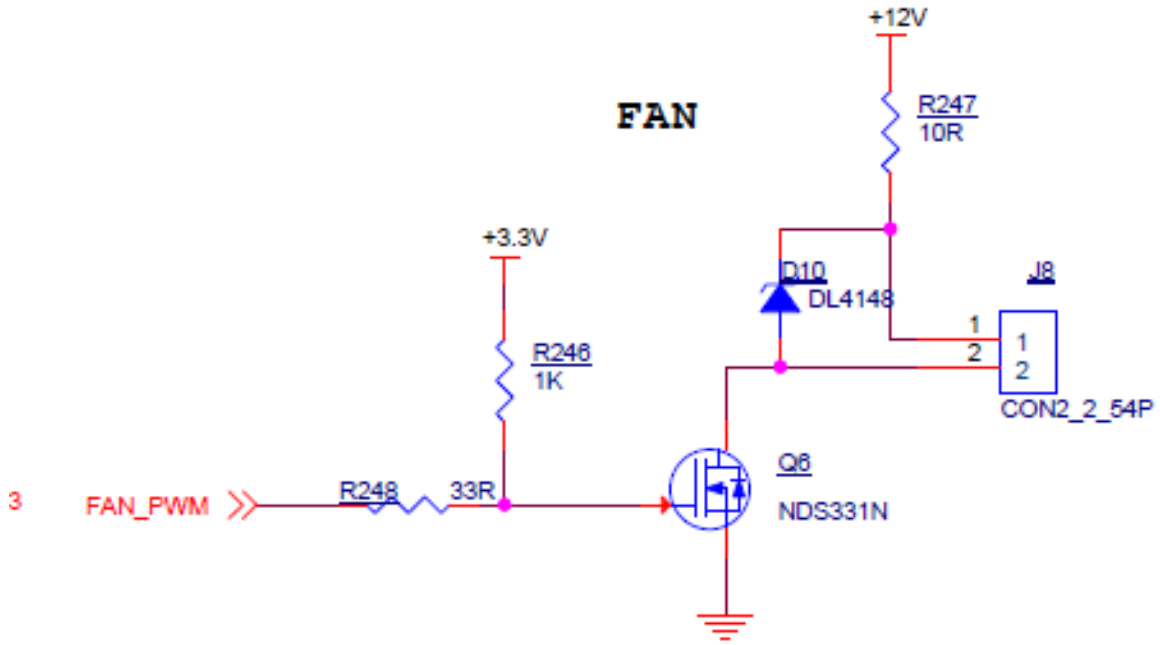


Figure 19-1：Fan design in the AX7350 FPGA Board schematic

The fan has been screwed to the AX7450 FPGA development board before leaving the factory. The power of the fan is connected to the socket of J8. The red is positive and the black is negative.

Part 20: Dimensional structure

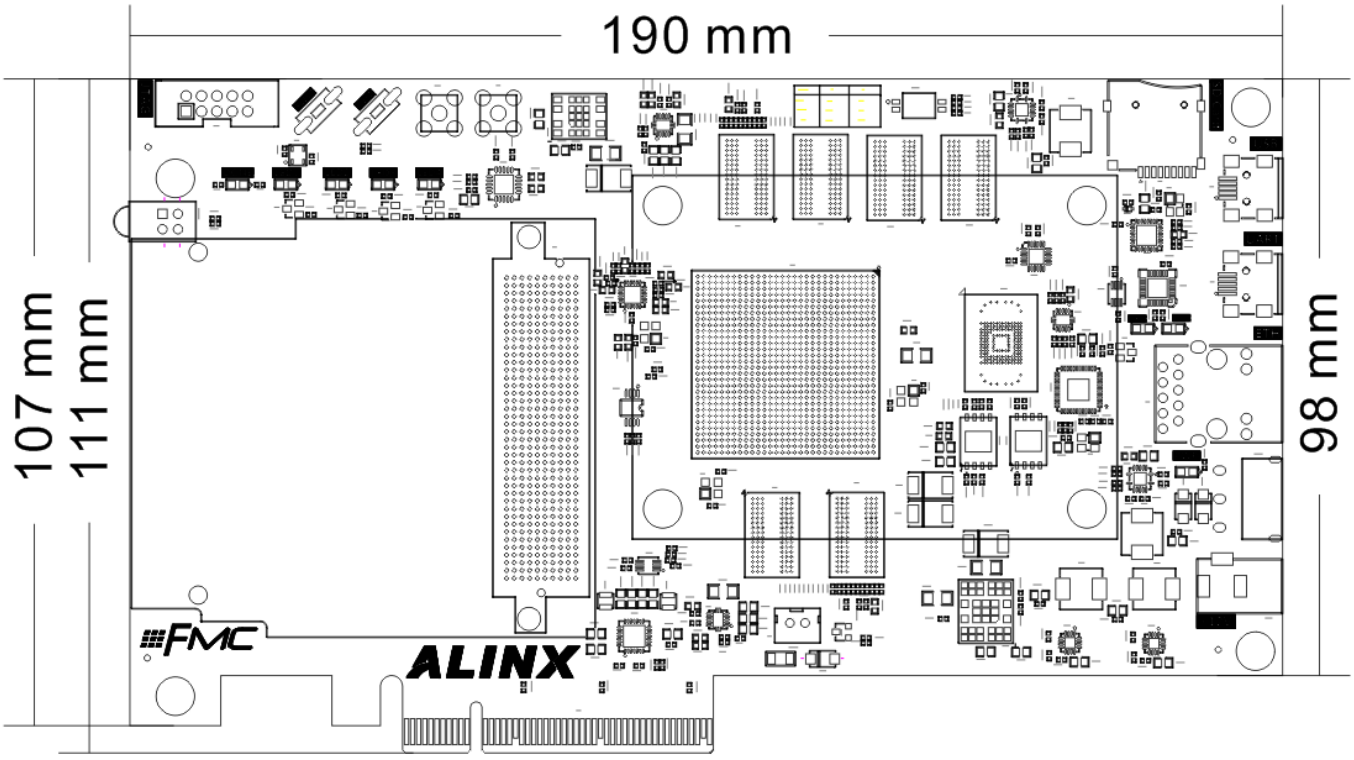


Figure 20-1: Top View