Cyclone IV FPGA Development Board AX530 User Manual

ALINX

Version Record

Version	Date	Release By	Description
Rev 1.0	2019-04-30	Rachel Zhou	First Release

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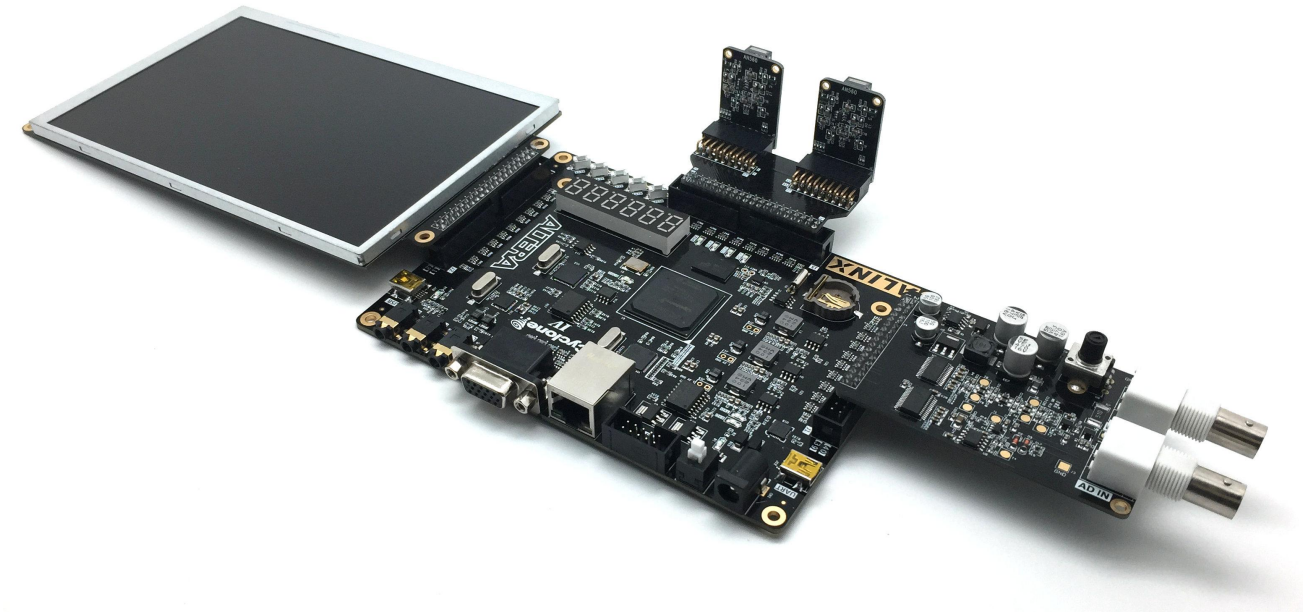
The FPGA development board (AX530) is an entry-level product, mainly for FPGA beginners. The FPGA development board uses the ALTERA CYCLONE IV family chips, model EP4CE30F23C8, in a 484-pin FBGA package. The AX530 FPGA development board has a wealth of hardware resources and peripheral interfaces. In the design, adhere to the "exquisite, practical, simple" design concept, it is very suitable for software radio, industrial control, multimedia applications, IC verification, parallel computing and other project development, and it can also be applied to college teaching, FPGA training, personal research learning and DIY etc.



Part 1: FPGA Development Board Introduction

This development board uses ALTERA CYCLONE IV series FPGA, model EP4CE30F23C7, 484-pin FBGA package. The resources of this FPGA are shown below:

Resources	EP4CE6	EP4CE10	EP4CE15	EP4CE22	EP4CE30	EP4CE40	EP4CE55	EP4CE75	EP4CE115
Logic elements (LEs)	6,272	10,320	15,408	22,320	28,848	39,600	55,856	75,408	114,480
Embedded memory (Kbits)	270	414	504	594	594	1,134	2,340	2,745	3,888
Embedded 18 × 18 multipliers	15	23	56	66	66	116	154	200	266
General-purpose PLLs	2	2	4	4	4	4	4	4	4
Global Clock Networks	10	10	20	20	20	20	20	20	20
User I/O Banks	8	8	8	8	8	8	8	8	8
Maximum user I/O (1)	179	179	343	153	532	532	374	426	528

Table 1-1: The Feature Summary of FPGA Device

The main resources and features are listed (see Table 1-2):

Parameter	Value
Logic elements (LEs)	28848
Embedded memory (Kbits)	594
Embedded 18 x18 multipliers	66
General-purpose PLLs	4
Global Clock Networks	20
User I/O Banks	8
Maximum User I/O	532

Table 1-1: The Main Resources and Feature of ALTERA EP4CE30

The layout of the board that indicates the location of the connector and key components, provide a quickly overview of AX530 board (see Figure 1-2)

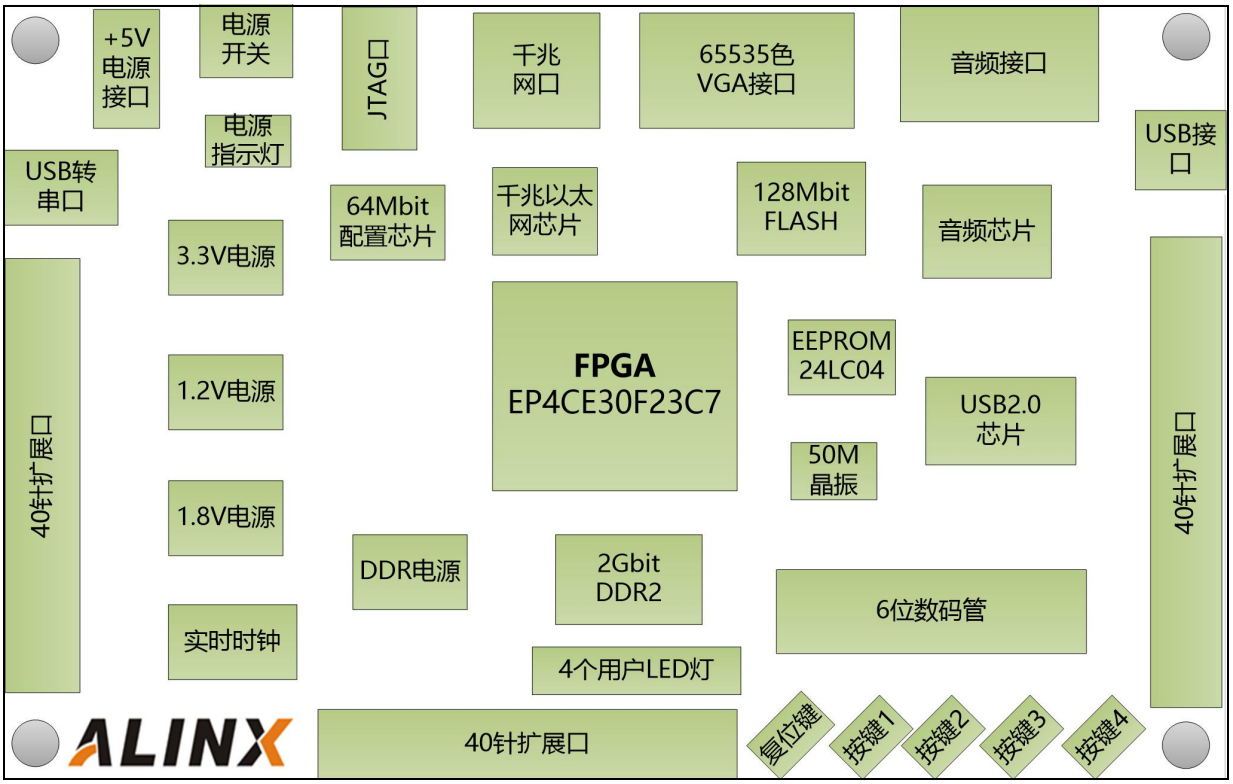


Figure 1-2: The Layout of the AX530

Through this diagram, we can see the functions that the development platform can achieve.

- +5V power input, maximum 2A current protection
- A large-capacity 2Gbit high-speed DDR2 SDRAM can be used as a data cache or as a memory for NIOS II operation;
- A 64Mbit configuration chip EPCS64 (actually soldered to M25P64, select EPCS64 when building project selection), can be used as storage for FPGA configuration files
- A 256Mbit QSPI FLASH that can be used as a storage for FPGA user data
- One-way 10/100M/1000M Ethernet RJ-45 interface for Ethernet data exchange with computers or other network devices;

- One-way high-speed USB2.0 interface, can be used for USB2.0 high-speed communication between FPGA development board and PC;
- One USB Uart interface for serial communication with PC or external devices
- One-port VGA interface, VGA interface is 16bit, can display 65,536 colors, can display color pictures, etc
- A high-quality audio interface that enables audio capture and output functions;
- A piece of RTC real time clock with battery holder, battery model CR1220
- One piece of IIC interface EEPROM 24LC04
- 4 red user LEDs
- 4 independent user buttons
- On-board 50M active crystal oscillator provides stable clock source for FPGA development board
- 3-Way 40-pin ALINX expansion port (0.1 inch), each expansion port with 34 IO ports, one 5V power supply, two 3.3V power supplies, three GND. Two expansion modules can be connected at the same time, such as expansion modules such as 4.3-inch TFT module and AD/DA module.
- Reserved JTAG port for FPGA debugging and program curing
- One way Micro SD card slot, Support SD mode and SPI mode
- Reserve a 2.5V power supply, which is Optional FPGA IO voltage 3.3V and 2.5V

Part 2: Structure Diagram

The size of the development board is a compact 130mm x 90mm, and the PCB is designed with a 6-layer board. There are 4 screw positioning holes

around the FPGA board for fixing the development board. The hole diameter of the positioning hole are 3.3mm (diameter)

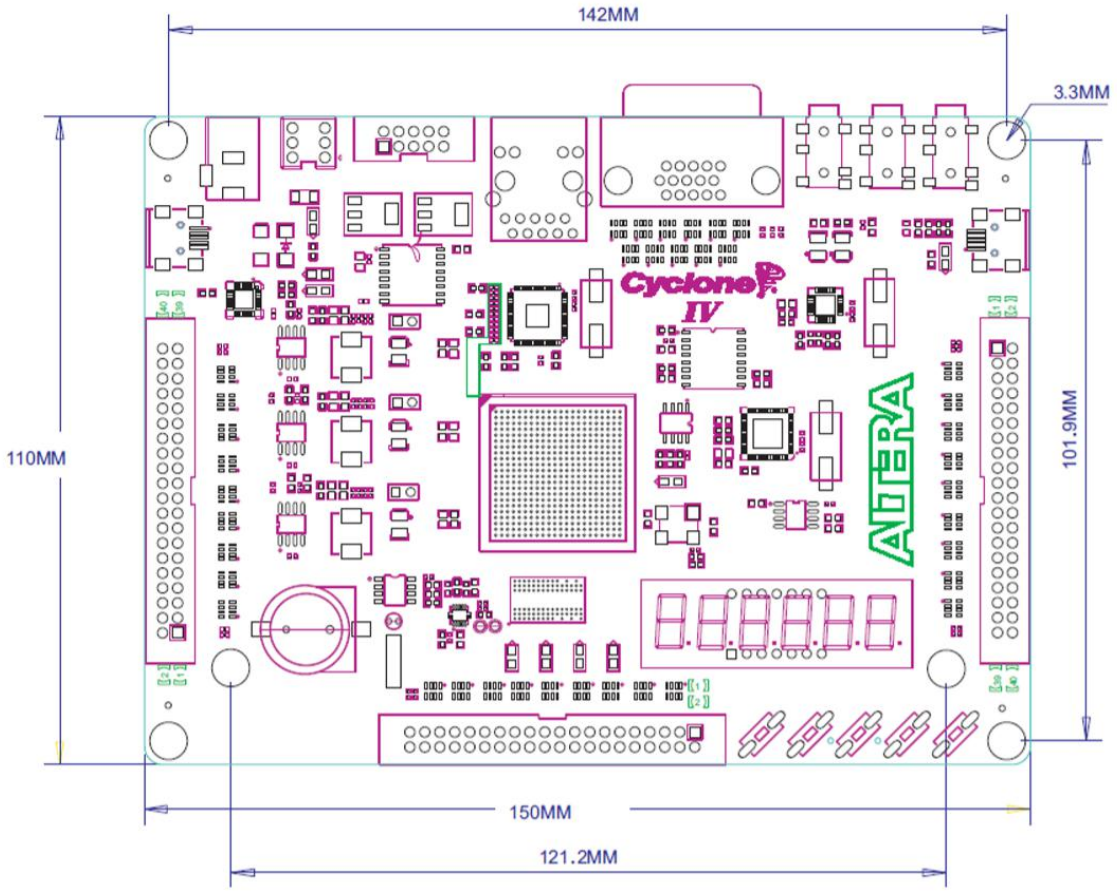


Figure 2-1: Structure Diagram

Part 3: Power

The power supply voltage of the AX530 FPGA development board is DC5V, and Figure 3-1 is the power supply schematic:

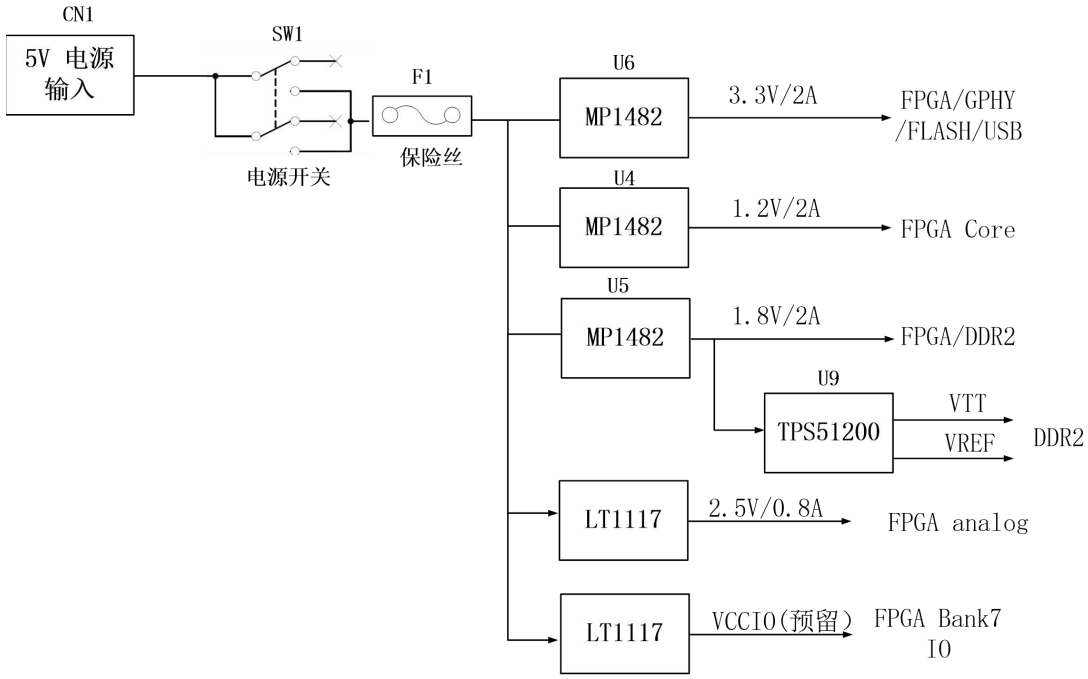


Figure 3-1: Block Diagram of Power Design

The FPGA development board is powered by +5V, and is converted into +3.3V, +1.2V, +1.8V three-way power supply through three-way DC/DC power supply chip MP1482, and generates +2.5V power supply and VCCIO (2.5V) through two LDO LT1117. The 1.8V generates the VTT and VREF voltages required by DDR2 through TPS51200 of TI. The functions of each power distribution are shown in the following table:

Power Supply	Function
+3.3V	FPGA, Gigabit Ethernet, Serial Port, RTC, Flash, EEPROM, USB 2.0, SD Card
+1.2V	FPGA Core
+1.8	DDR2, FPGA Bank3 Bank4
+2.5V	FPGA Analog Power
VREF, VTT	0.9V, DDR2 reference voltage and termination voltage
VCCIO	2.5V, FPGA Bank7 optional

The IO voltage of FPGA BANK7 can be selected by two 0 ohm resistors (R158, R159) on the FPGA development board. When R158 is installed and R159 is not installed, the IO level of Bank7 is 3.3V. When R158 is not installed, R159 is installed. At the time, the IO level of Bank 7 is 2.5V.

FPGA BANK voltage distribution:

BANK	Function	Voltage	Description
BANK1	1000M Ethernet	3.3V	
BANK2	Expansion header J1	3.3V	
BANK3	DDR2	1.8V	
BANK4	DDR2	1.8V	
BANK5	Digital tube, Expansion header J3	3.3V	
BANK6	USB、SD card slot	3.3V	
BANK7	LED，Expansion header J2	3.3V/2.5V	IO voltage is adjustable
BANK8	Audio、EEPROM、VGA、RTC、UART	3.3V	

In the PCB design, the 6-layer PCB is used, and a separate power supply layer and GND layer are reserved, so that the power supply of the entire development board has very good stability. Test points for each power supply are reserved on the PCB so that the user can confirm the voltage on the board.

Part 4: FPGA Chip

As mentioned earlier, the FPGA model we use is EP4CE30F23C8, which belongs to ALTERA CYCLONE IV. This model is a FBGA package with 484 pins. Again, explain the definition of the FPGA pin. Many people use FPGAs that are not BGA-packaged, such as 144-pin, 208-pin FPGA chips. Their pin definitions are made up of numbers, such as 1 to 144, 1 to 208, etc., and when we use

BGA packages. After the chip, the pin name becomes in the form of letters + numbers, such as E3, G3, etc., so when we look at the schematic, we see the letters + numbers, which represent the pins of the FPGA. Having said this, let's look at the functions of the various parts of the FPGA.

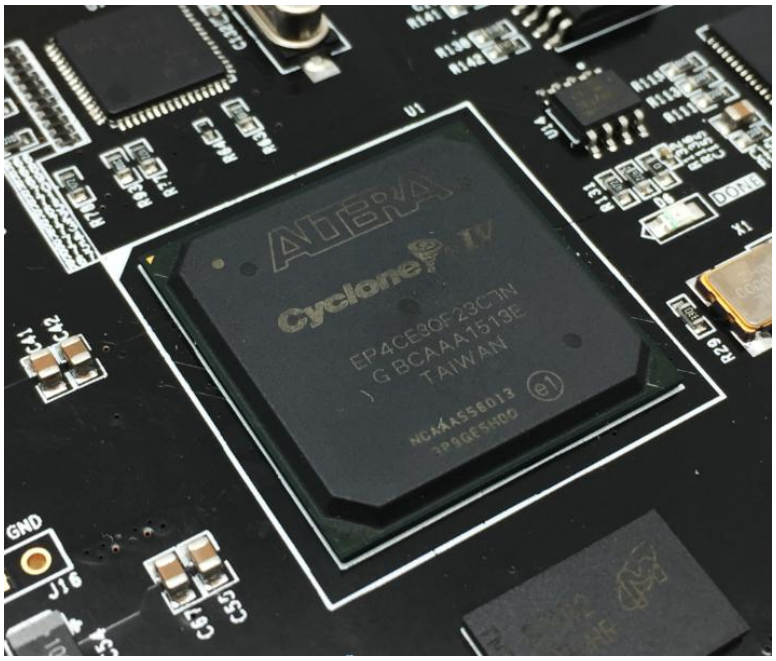


Figure 4-1: FPGA Chip on the FPGA Board

Part 4.1: FPGA resources

The EP4CE30F23C8 chip contains logic resources, built-in RAM, multiplier, phase-locked loop, global clock network and IO port. The resources between different types of FPGAs will be different. The resources of the FPGA model on the AX530 development board are shown in Figure 4-2 below

Resources	EP4CE6	EP4CE10	EP4CE15	EP4CE22	EP4CE30	EP4CE40	EP4CE55	EP4CE75	EP4CE115
Logic elements (LEs)	6,272	10,320	15,408	22,320	28,848	39,600	55,856	75,408	114,480
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Global Clock Networks	10	10	20	20	20	20	20	20	20
User I/O Banks	8	8	8	8	8	8	8	8	8
Maximum user I/O (1)	179	179	343	153	532	532	374	426	528

Figure 4-2：FPGA internal resources

Part 4.2: JTAG Interface

First let's talk about the FPGA configuration and debugging interface: JTAG interface. The function of the JTAG interface is to download the compiled program (.sof) to the FPGA or download the configuration file (.jic) to the configuration chip EPCS64. After the sof file is downloaded to the FPGA, it will be lost after power-off. Re-download it. However, the JIC file that is solidified into the configuration chip will not be lost after power-off. After power-on, the FPGA will read the configuration file in the configuration chip EPCS64 and run it. Figure 3-3 is the schematic part of the JTAG port, which involves the four signals TCK, TDO, TMS, TDI.

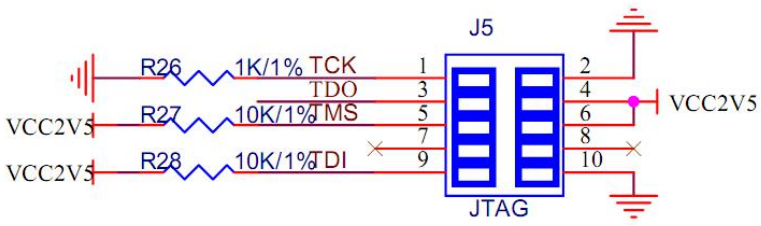

Figure 4-3： JTAGE Schematic

The JTAG interface uses a 10-pin 2.54mm standard connector, and Figure 4-4 shows the JTAG interface on the FPGA development board.

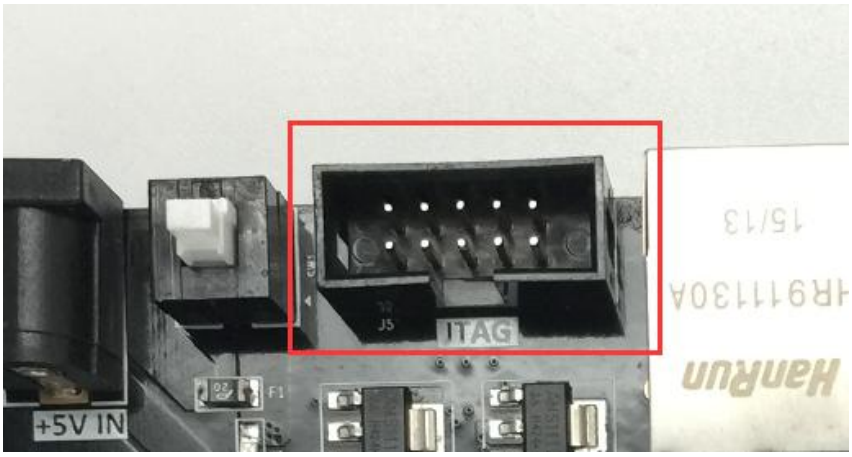

Figure 4-4: JTAG Connector on the FPGA board

Part 4.3: FPGA Power Supply

Next, let's talk about the power supply pin part of the FPGA, where VCCIO is the power supply pin of the Bank, which determines the level of the IO port corresponding to each BANK. As shown in Figure 3-5, Bank1, Bank2, Bank5, Bank6, Bank8 is connected to VCC3V3. The corresponding IO level of these banks is 3.3V. Bank3 and Bank4 are connected to DDR2. The required IO is 1.8V, so we are connected to VCC1V8. Bank7 we set it to VCCIO7, where we can choose the voltage according to our own needs, the default is 3.3V. Change the resistance of R158 to R159 and change the BANK7 voltage to 2.5V. If there are other requirements, different voltages can be achieved by replacing the power supply chip U19.

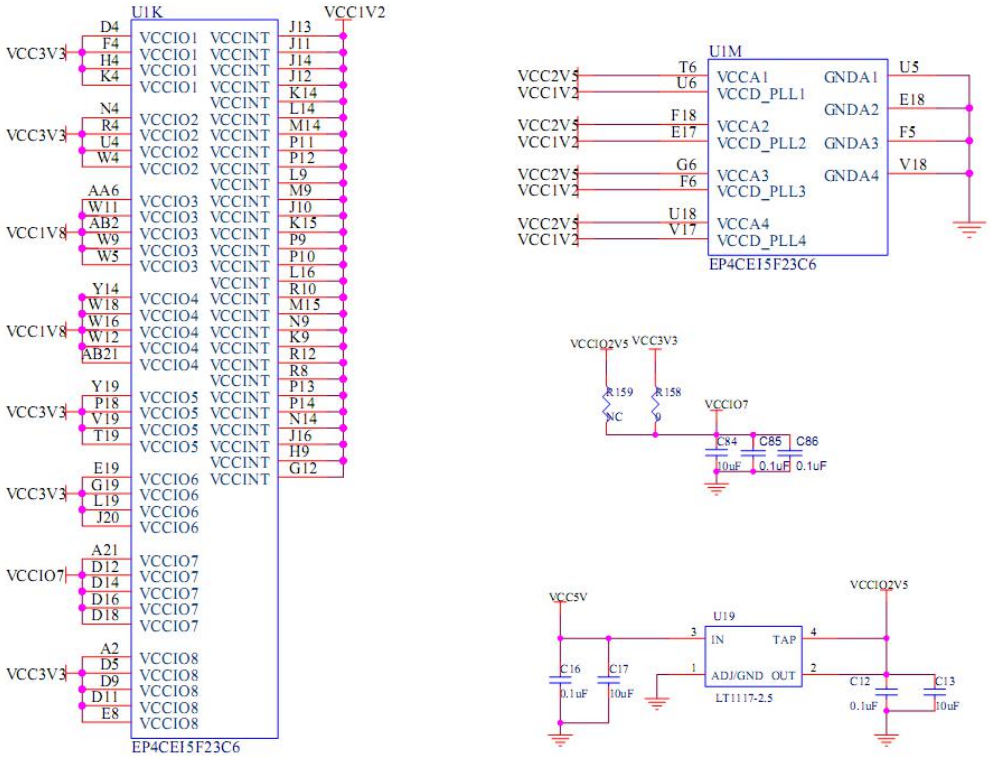

Figure 4-5: FPGA Power Supply

Part 5: 50Mhz Clock

Figure 5-1 is the 50M active crystal oscillator circuit mentioned above that provides the clock source for the FPGA development board. The crystal output is connected to the global clock (GCLK Pin T21) of the FPGA, which can be used to drive the user logic within the FPGA. The user can configure the internal PLLs of FPGA to achieve a higher clock.

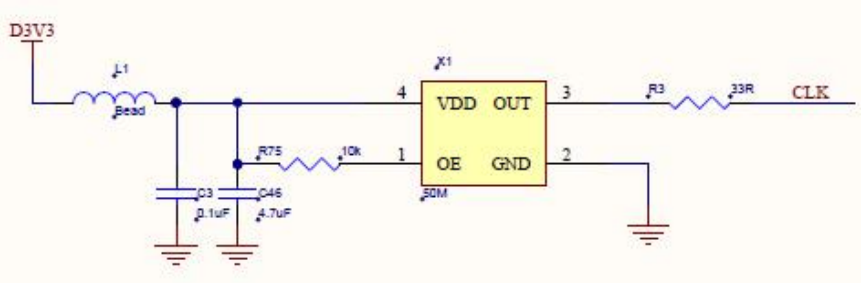

Figure 5-1: 50Mhz Crystal Oscillator

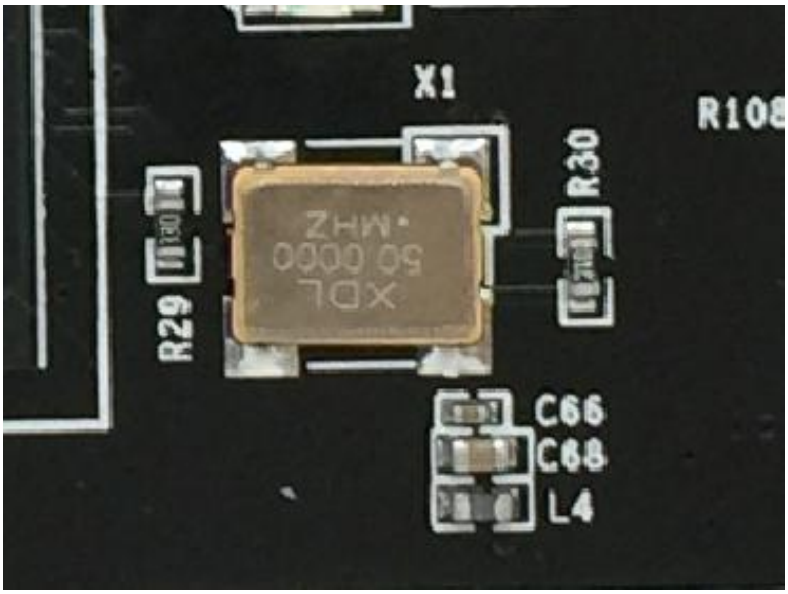

Figure 5-2: 50Mhz crystal oscillator on the FPGA Development Board

Clock Pin Assignment

Net Name	FPGA PIN
CLK	T21

Part 6: SPI Flash Configuration chip

A 64Mbit configuration chip is used on the development board, the model is M25P64. This chip is fully compatible with the configuration chip EPCS64. When we make the configuration chip selection, we can directly select EPCS64. Due to its non-volatile nature, the configuration chip can be used as a storage device for storing configuration information of the FPGA system during use, and can also save information content when power is off. When power is restored, the configuration chip EPCS64 transfers the configuration information to the FPGA and then runs.

The specific models and related parameters of SPI FLASH are shown in Table 6-1

Part	Device	Size	Manufacturer
U7	M25P16VMF	64M bit	ST

Table 6-1: The model of SPI Flash and Parameters

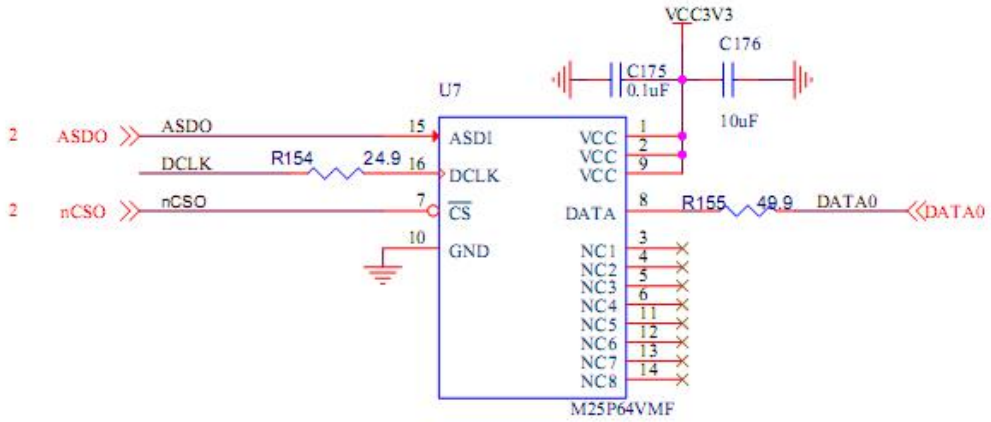

Figure 6-1: The Hardware Design of SPI FLASH

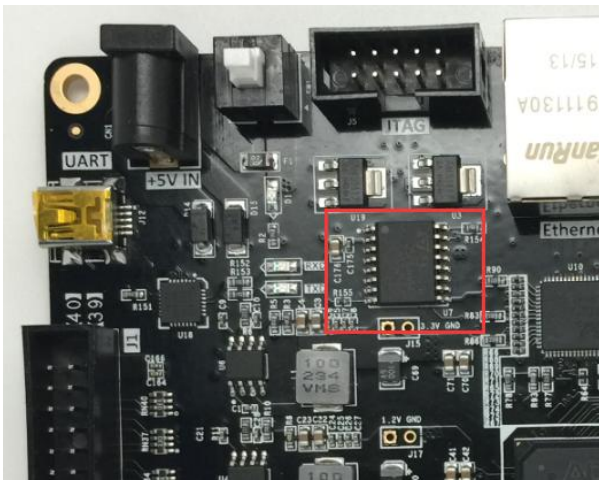

Figure 6-2: EPCS64(M25P64) on the FPGA board

Configure chip pin assignments:

Pin Name	FPGA Pin
ASDO	D1
DCLK	K2
nCSO	E2
DATA0	K1

Part 7: QSPI Flash

The AX530 FPGA development board is equipped with a 128MBit Quad-SPI FLASH chip, model W25Q128, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, In use, QSPI FLASH can be used as power-down storage for user data. It mainly includes user data, image information and system files, and so on. The specific models and related parameters of QSPI FLASH are shown in Table 7-1.

Position	Model	Capacity	Factory
U17	W25Q128BV	128M Bit	Winbond

Table 7-1: QSPI FLASH Specification

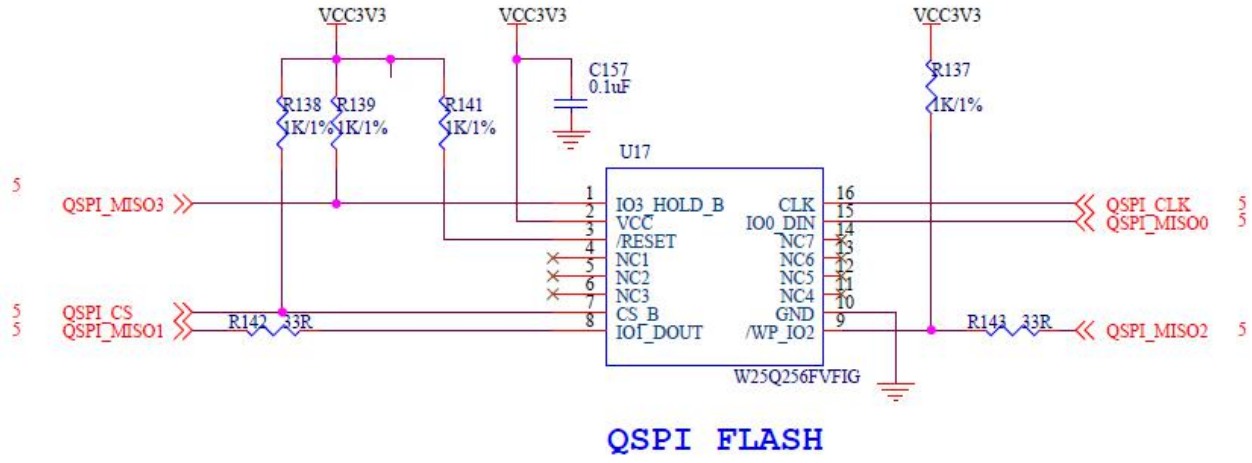

Figure 7-1: QSPI Flash Schematic

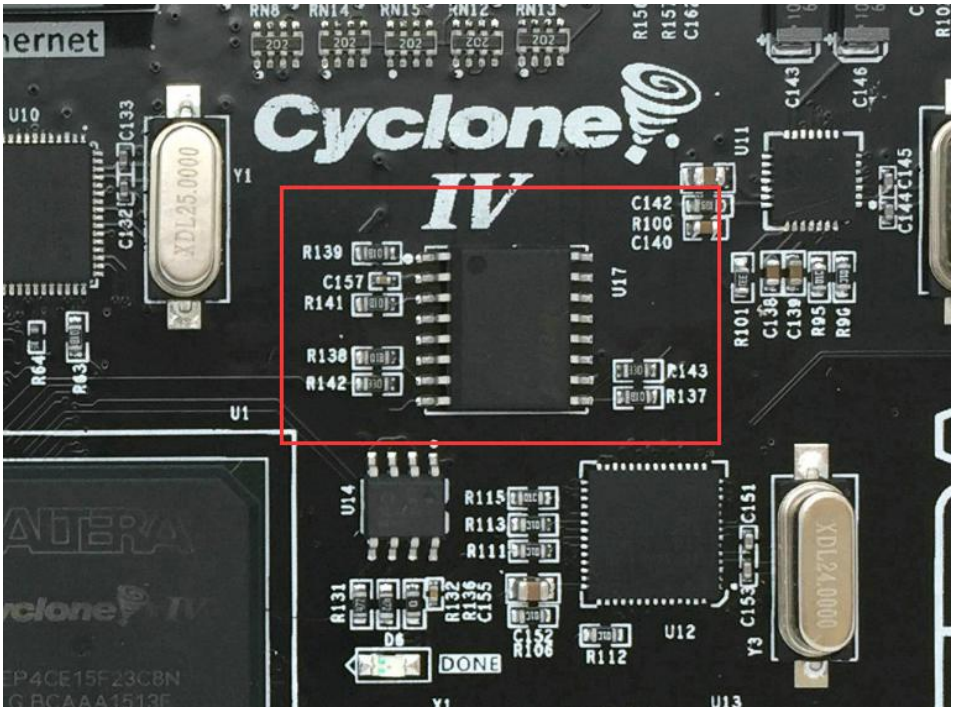

Figure 7-2: QSPI Flash chip on the FPGA board

Configure chip pin assignments:

Pin Name	FPGA Pin
QSPI_CLK	A7
QSPI_CS	A6
QSPI_MISO0	B7
QSPI_MISO1	B6
QSPI_MISO2	E9
QSPI_MISO3	B8

Part 8: DDR2 DRAM

The development board contains a high-speed DDR2 DRAM, model: MT47H128M16HR-3IT, capacity: 2Gbit (128M*16bit), 16bit bus. The FPGA and DDR2 DRAM on the development board are connected to the IO of BANK3 and BANK4, and the level is 1.8V. The clock frequency between the FPGA and

DDR2 is up to 166.7MHz, and the data frequency is up to 333MHz. The hardware design of DDR2 requires strict consideration of signal integrity. In the circuit design and PCB design, the matching resistor/terminal resistor, trace impedance control, and trace length control have been fully considered to ensure the high-speed stability of DDR2.

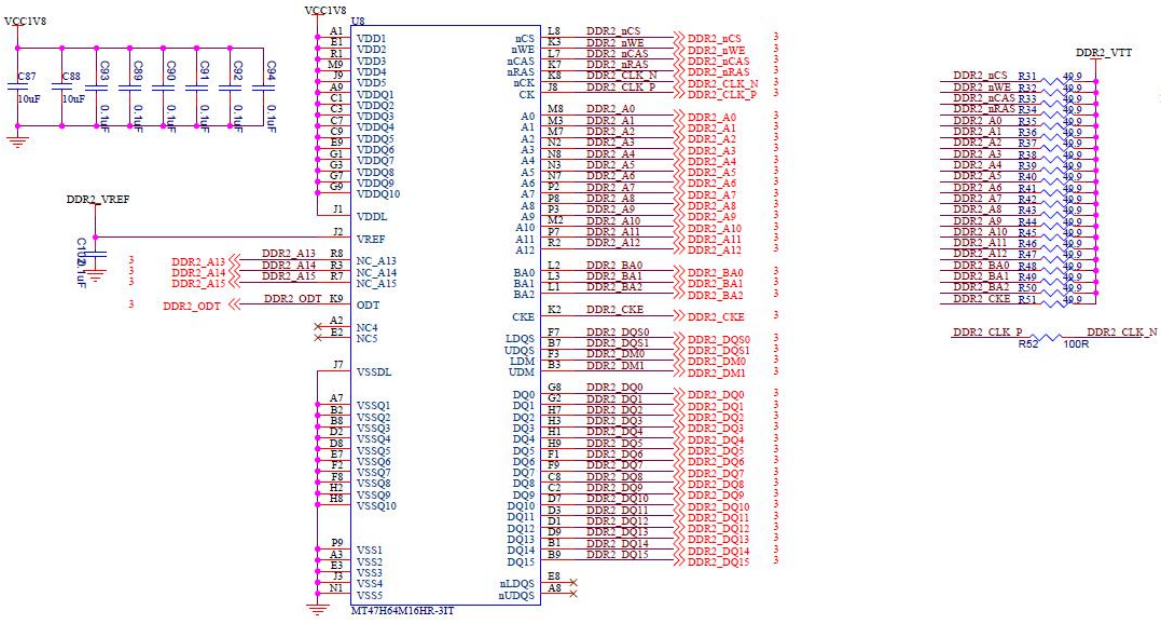

Figure 8-1: DDR2 DRAM Schematic

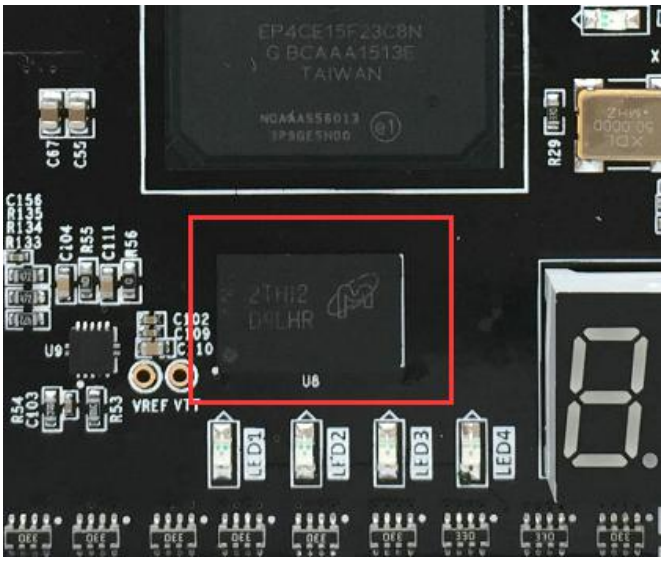

Figure 8-2: DDR2 DRAM on the FPGA Board

DDR2 DRAM Pin Assignment:

Pin Name	FPGA Pin
DDR2_DQS[0]	AB9
DDR2_DQS[1]	V10
DDR2_DQ[0]	AB8
DDR2_DQ [1]	Y8
DDR2_DQ [2]	AA9
DDR2_DQ [3]	W10
DDR2_DQ [4]	V11
DDR2_DQ [5]	Y10
DDR2_DQ [6]	AB7
DDR2_DQ [7]	AA8
DDR2_DQ [8]	Y7
DDR2_DQ [9]	U9
DDR2_DQ [10]	V8
DDR2_DQ [11]	W6
DDR2_DQ [12]	W7
DDR2_DQ [13]	W8
DDR2_DQ [14]	Y3
DDR2_DQ [15]	AA5
DDR2_DM[1]	V5
DDR2_DM[0]	AA7
DDR2_A[0]	V6
DDR2_A [1]	U13
DDR2_A [2]	V7
DDR2_A [3]	T14
DDR2_A [4]	U7
DDR2_A [5]	U15
DDR2_A [6]	U8
DDR2_A [7]	R16
DDR2_A [8]	U10
DDR2_A [9]	R14
DDR2_A [10]	U14

DDR2_A [11]	T9
DDR2_A [12]	R15
DDR2_A [13]	T10
DDR2_A [14]	T16
DDR2_BA [0]	Y17
DDR2_BA [1]	W15
DDR2_BA [2]	V15
DDR2_RAS_N	AA4
DDR2_CAS_N	AB10
DDR2_WE_N	AA3
DDR2_ODT	AB5
DDR2_CLK	AA17
DDR2_CLK_N	AB17
DDR2_CKE	AB3
DDR2_CS_N	Y6

Part 9: EEPROM 24LC04

The development board contains an EEPROM, model 24LC04, and its capacity is 4Kbit (2*256*8bit). It consists of two 256-byte blocks and communicates via the IIC bus. The onboard EEPROM is to learn the communication method of the IIC bus. EEPROM is generally used in the design of instruments and meters, used as storage of some parameters, power loss is not lost. This chip is easy to operate and has a very high price/performance ratio, so although the capacity is relatively small, the price is very cheap, which is a good choice for those products that are costly.

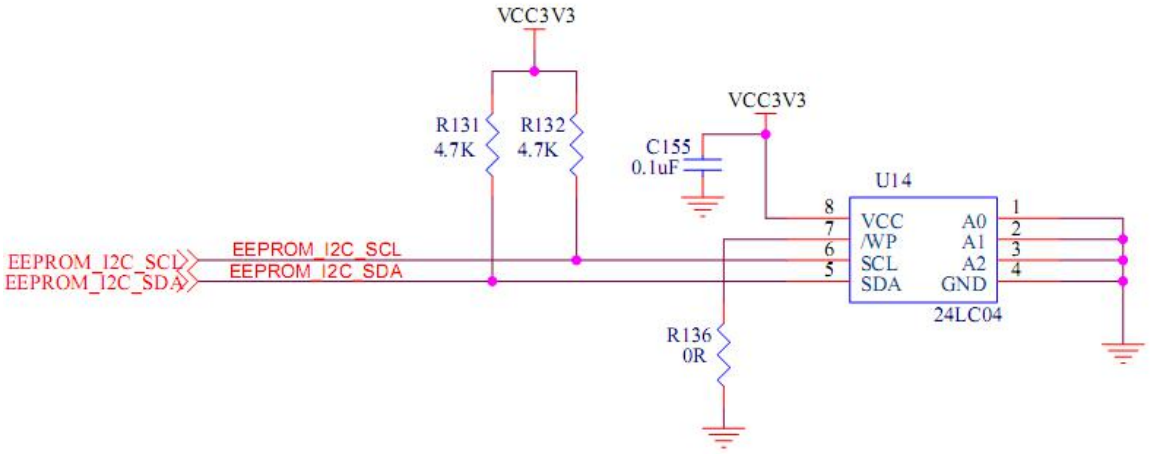

Figure 9-1: EEPROM Design

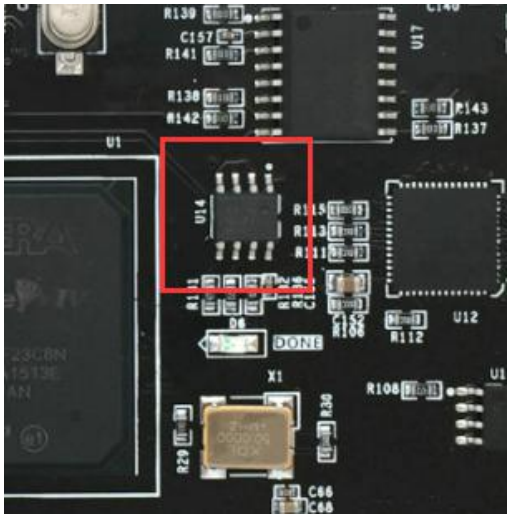

Figure 9-2: EEPROM on the AX515 FPGA board

EEPROM PIN assignment:

Net Name	FPGA PIN
EEPROM_I2C_SDA	A8
EEPROM_I2C_SCL	G11

Part 10:Real-Time Clock

The FPGA development board contains a real-time clock RTC chip, model

DS1302. Its function is to provide the calendar function to 2099, with days, minutes, minutes, seconds and weeks. If time is required in the system, the RTC needs to be designed into the product. He needs to connect a 32.768KHz passive clock to provide an accurate clock source to the clock chip, so that the RTC can accurately provide clock information to the product. At the same time, in order to power off the product, the real-time clock can still run normally. Generally, a battery is required to supply power to the clock chip. In Figure 8.1, U7 is the battery holder. We put the button battery (model CR1220, voltage is 3V) into the battery. When the system is powered off, the button battery can also supply power to the DS1302, so that regardless of whether the product is powered or not, the DS1302 will operate normally without interruption and provide continuous time information. Figure 10-1 shows the schematic of the DS1302:

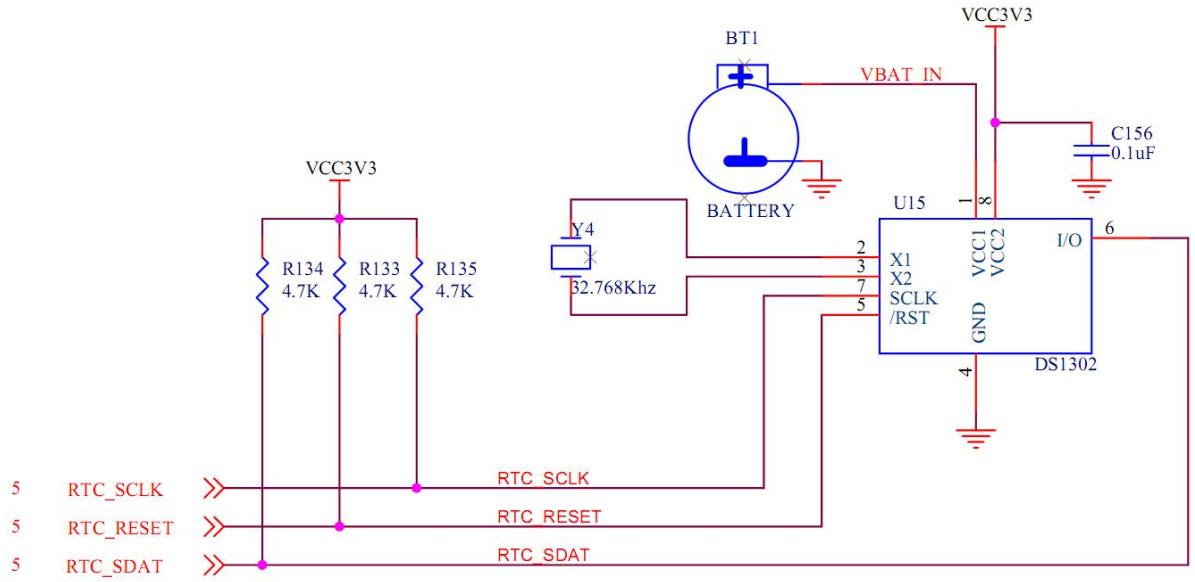

Figure 10-1: RTC Hardware Design

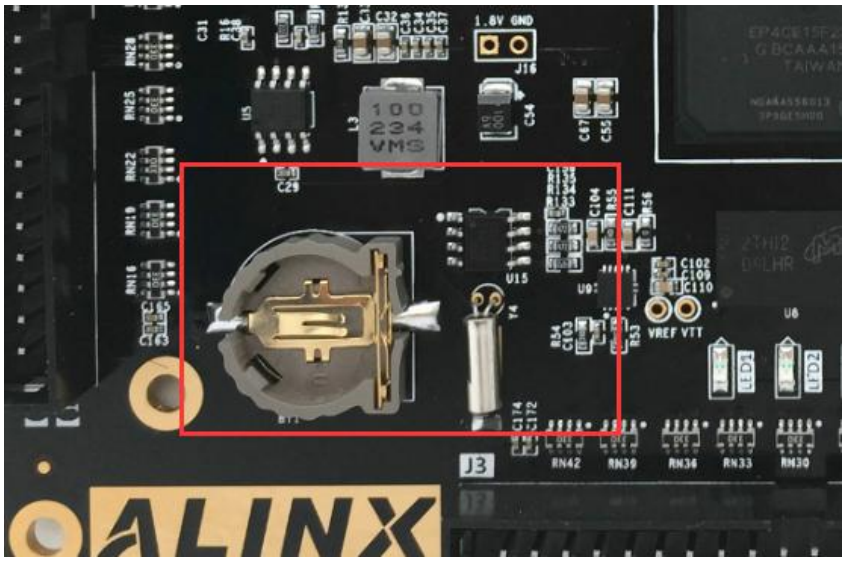

Figure 10-2: DS1302 Circuit on FPGA board

DS1302 Interface Pin Assignment:

Net Name	FPGA PIN
RTC_SIO	E6
RTC_RESET	G9
RTC_SCLK	E5

Part 11: Gigabit Ethernet Interface

The AX530 FPGA development board provides network communication services to users through the Realtek RTL8211EG Ethernet PHY chip. The RTL8211EG chip supports 10/100/1000 Mbps network transmission rate and communicates with the FPGA through the GMII interface. RTL8211EG supports MDI/MDX adaptive, various speed adaptations, Master/Slave adaptation, and support for MDIO bus for PHY register management.

The RTL8211EG will detect the level status of some specific IOs to determine their working mode after powered on. Table 11-1 describes the default setup information after the GPHY chip is powered on.

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address 011
SELRGV	3.3V, 2.5V, 1.5/1.8V voltage selection	3.3V
AN[1:0]	Auto-negotiation configuration	(10/100/1000M) adaptive
RX Delay	RX clock 2ns delay	Delay
TX Delay	TX clock 2ns delay	Delay
Mode	RGMII or GMII selection	GMII

Table 11-1: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of FPGA and PHY chip RTL8211EG is communicated through the GMII bus, the transmission clock is 125Mhz. The receive clock E_RXC is provided by the PHY chip, the transmit clock E_GTXC is provided by the FPGA, and the data is sampled on the rising edge of the clock.

When the network is connected to 100M Ethernet, the data transmission of FPGA and PHY chip RTL8211EG is communicated through the MII bus, the transmission clock is 25Mhz. The receive clock E_RXC is provided by the PHY chip, the transmit clock E_GTXC is provided by the FPGA, and the data is sampled on the rising edge of the clock.

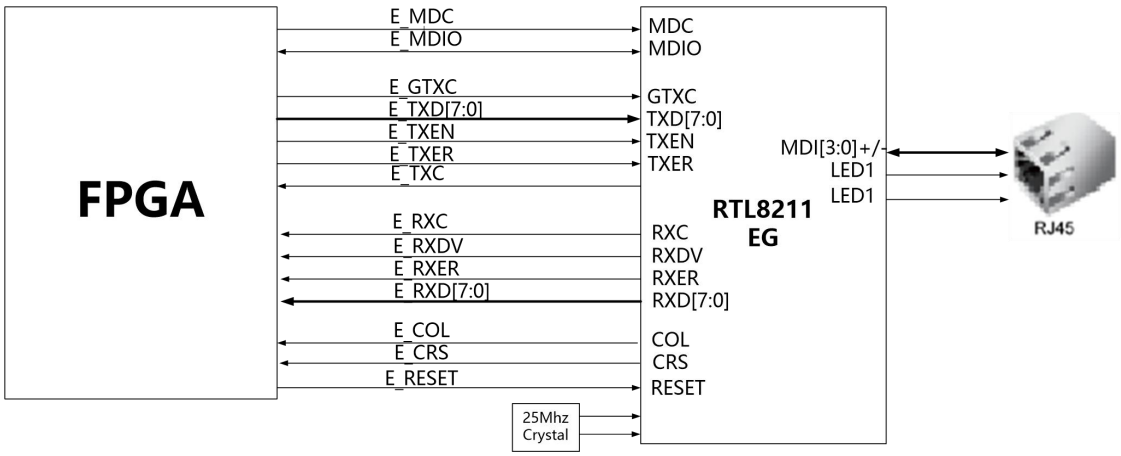

Figure 11-1: FPGA and PHY connection diagram

Figure 11-2: Ethernet PHY chip on the FPGA board

Gigabit Ethernet pin assignments are as follows：

Signal Name	FPGA Pin	Description
E_GCLK	H1	Ethernet GMII transmit clock
E_TXD0	F2	Ethernet Transmit Data bit0
E_TXD1	E1	Ethernet Transmit Data bit1
E_TXD2	G4	Ethernet Transmit Data bit2
E_TXD3	J1	Ethernet Transmit Data bit3
E_TXD4	H5	Ethernet Transmit Data bit4
E_TXD5	J3	Ethernet Transmit Data bit5
E_TXD6	K7	Ethernet Transmit Data bit6
E_TXD7	J7	Ethernet Transmit Data bit7
E_TXEN	G3	Ethernet transmit enable signal
E_TXER	L6	Ethernet transmit error signal
E_TXC	J4	Ethernet MII transmit clock
E_RXC	E3	Ethernet GMII receive clock
E_RXDV	J6	Ethernet receive data valid signal
E_RXER	B2	Ethernet receiving data error

E_RXD0	H6	Ethernet Receive Data Bit0
E_RXD1	G5	Ethernet Receive Data Bit1
E_RXD2	H7	Ethernet Receive Data Bit2
E_RXD3	E4	Ethernet Receive Data Bit3
E_RXD4	D2	Ethernet Receive Data Bit4
E_RXD5	C1	Ethernet Receive Data Bit5
E_RXD6	C2	Ethernet Receive Data Bit6
E_RXD7	B1	Ethernet Receive Data Bit7
E_COL	H2	Collision Signal
E_CRS	J2	Carrier Sense Signal
E_RESET	F1	Ethernet Reset Signal
E_MDC	K8	Ethernet Management Clock
E_MDIO	L8	Ethernet Management Data

Part 12: USB to Serial Port

The AX530 FPGA development board includes the USB-UAR chip of Silicon Labs CP2102GM. The USB interface uses the MINI USB interface. It can be connected to the USB port of the upper PC for serial data communication with a USB cable. The schematic diagram of the USB Uart circuit design is shown in Figure 12-1:

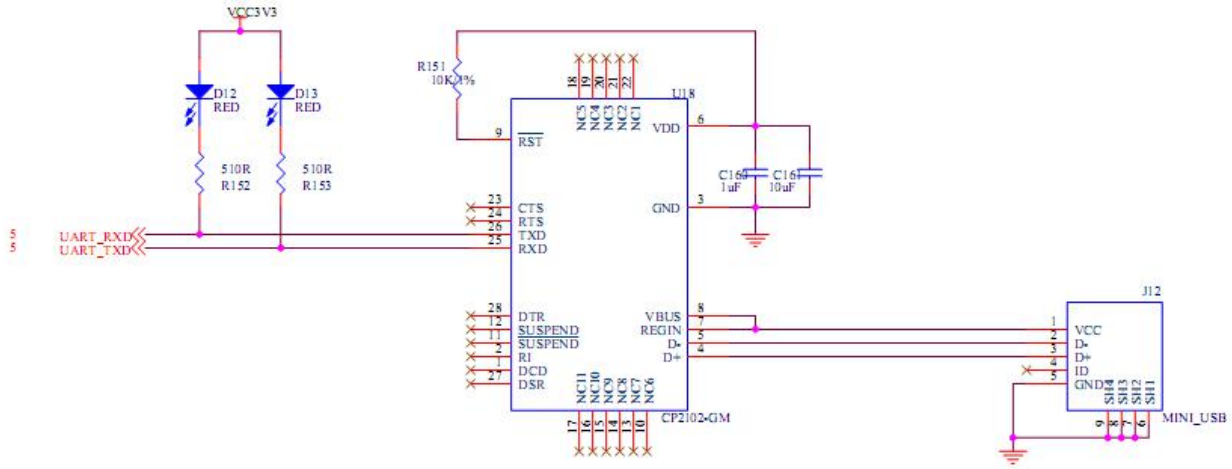

Figure 12-1: USB to Serial Port Schematic

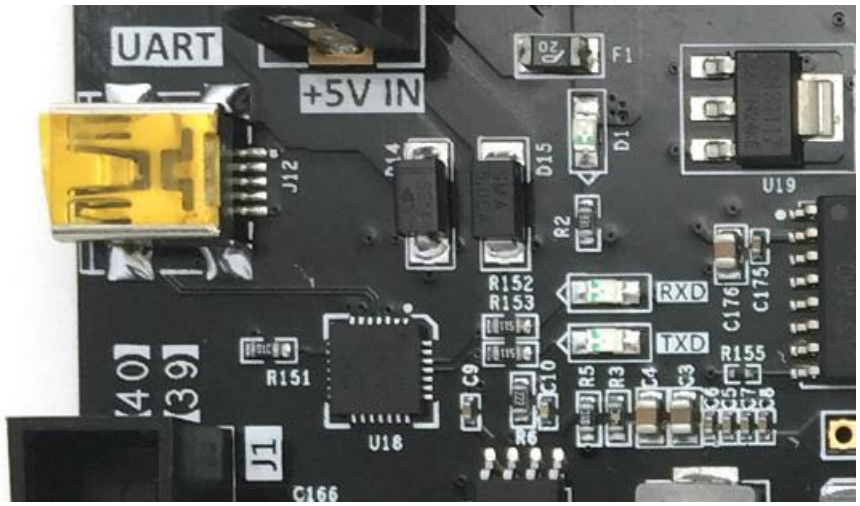

Figure 12-2: USB to Serial Port on the FPGA Board

At the same time, two LED indicators LED7 (RXD) and LED8 (TXD) are set for the serial port signal, and the silkscreen on the PCB is TX and RX, indicating that the serial port has data transmission or reception, as shown in the following Figure 12-3

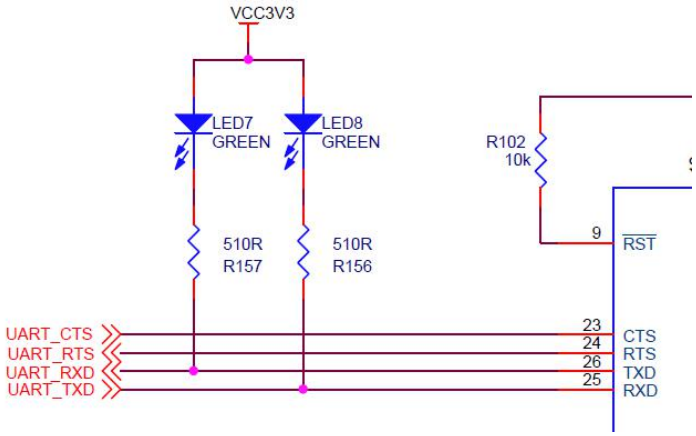

Figure 12-3: USB to Serial Port LED Indicator

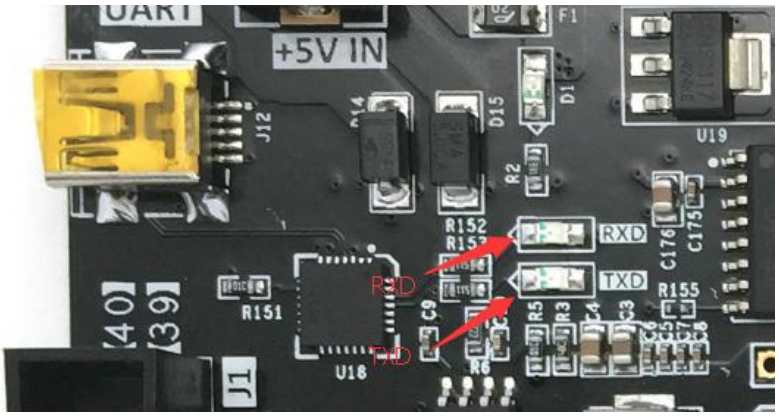

Figure 12-4: USB to Serial Port LED Indicator on FPGA Board

Serial Port Pin Assignment

Pin Name	FPGA Pin
UART_RXD	G7
UART_TXD	F9

Part 13: VGA Port

VGA interface, I believe many friends will not be unfamiliar, because this interface is the most important interface on the computer monitor. From the era of huge CRT monitors, the VGA interface has been used, and it has been used until now, and the VGA interface is also called For the D-Sub interface.

The VGA connector is a D-type connector with a total of 15 pinholes divided into three rows of five. More important are the three RGB color component signals and the two scan sync signals HSYNC and VSYNC pins.

Pins 1, 2, and 3 are red, green, and blue primary color analog voltages, which are 0 to 0.714V peak-peak, 0V is colorless, and 0.714V is full color. Some non-standard displays use a full color level of 1Vpp.

The three primary color source terminals and terminal matching resistors are both 75 ohms, detailed as Figure 13-1

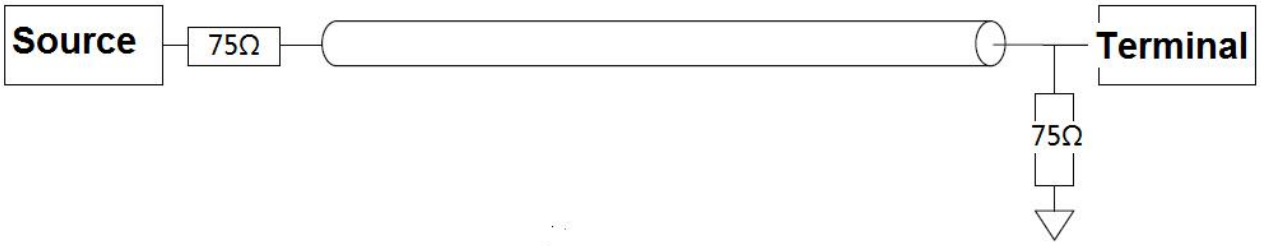

Figure 13-1: VGA video signal transmission diagram

HSYNC and VSYNC are line data synchronization and frame data synchronization, respectively, which are TTL levels. The FPGA can only output digital signals, while the R, G, and B required by VGA are analog signals. The digital to analog signal of VGA is realized by a simple resistor circuit. This resistor circuit can generate 32 gradient grade red and blue signals and 64 gradient grade green signals (RGB 5-6-5). Figure 13-2 detailed the VGA interface hardware design.

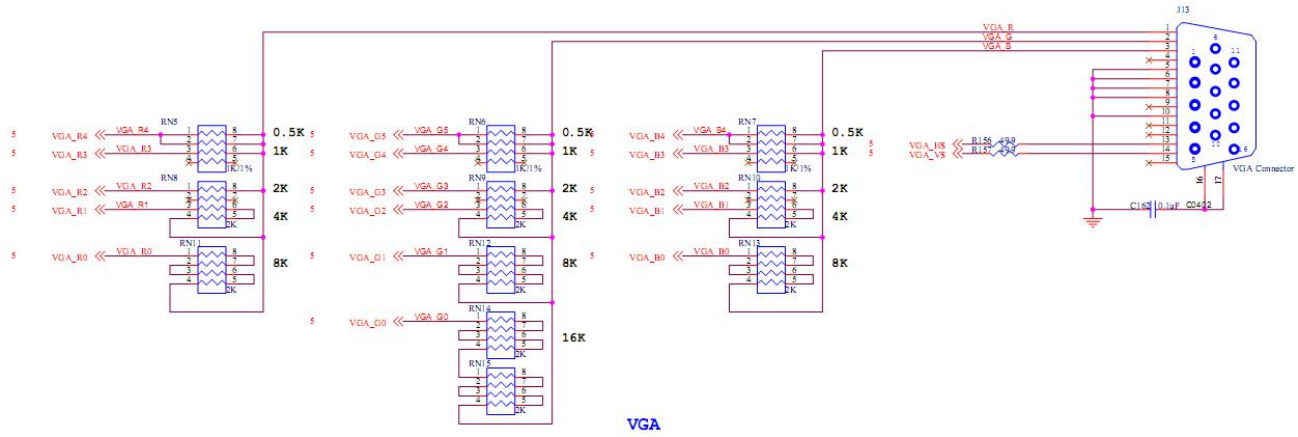

Figure 13-2: VGA Interface Hardware Design

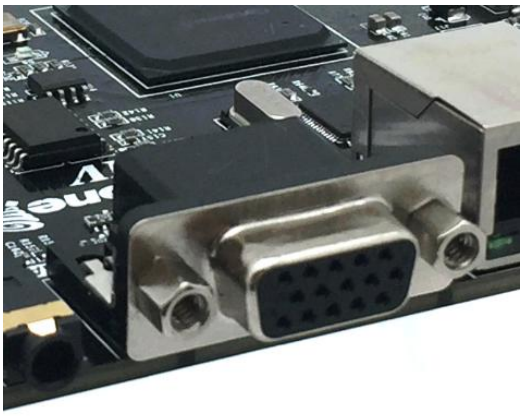

Figure 13-3: VGA Interface on board

VGA Interface Pin Assignment

Pin Name	FPGA Pin	Description
VGA_B[0]	G8	BLUE[0]
VGA_B[1]	G10	BLUE[1]
VGA_B[2]	F8	BLUE[2]
VGA_B[3]	C7	BLUE[3]
VGA_B[4]	F7	BLUE[4]
VGA_G[0]	B4	GREEN[0]
VGA_G[1]	E7	GREEN[1]
VGA_G[2]	C6	GREEN[2]
VGA_G[3]	D6	GREEN[3]
VGA_G[4]	A5	GREEN[4]
VGA_G[5]	B5	GREEN[5]
VGA_R[0]	B3	RED[0]
VGA_R[1]	C4	RED[1]
VGA_R[2]	A3	RED[2]
VGA_R[3]	A4	RED[3]
VGA_R[4]	C3	RED[4]
VGA_HS	F10	Horizontal sync signal
VGA_VS	H11	Vertical sync signal

Part 14: USB 2.0 interface

The FPGA development board uses Cypress CY7C68013A USB2.0 controller chip to realize high-speed data communication between PC and FPGA. CY7C68013A controller fully complies with the universal serial bus protocol version 2.0 specifications, supports full speed (12Mbit/s) and low speed (480Mbit/s) mode. The user can perform USB2.0 data communication by connecting the USB port of the PC with the USB cable and the MINI type USB port (J6) of the development board.

The CY7C68013A is a microcontroller with integrated USB 2.0. It integrates a USB 2.0 transceiver, SIE (serial interface engine), enhanced 8051 microcontroller and programmable external interface into a single chip. The communication between CY7C68013A and other devices is very simple. It provides GPIF and FIFO modes for seamless data exchange with FPGA, DSP, ATA, UTOPIA, EPP, PCMCIA etc.

The CY7C68013A transceiver is clocked by a 24MHz crystal oscillator. The schematic diagram of the FPGA and CY7C68013A connections is Figure 14-1:

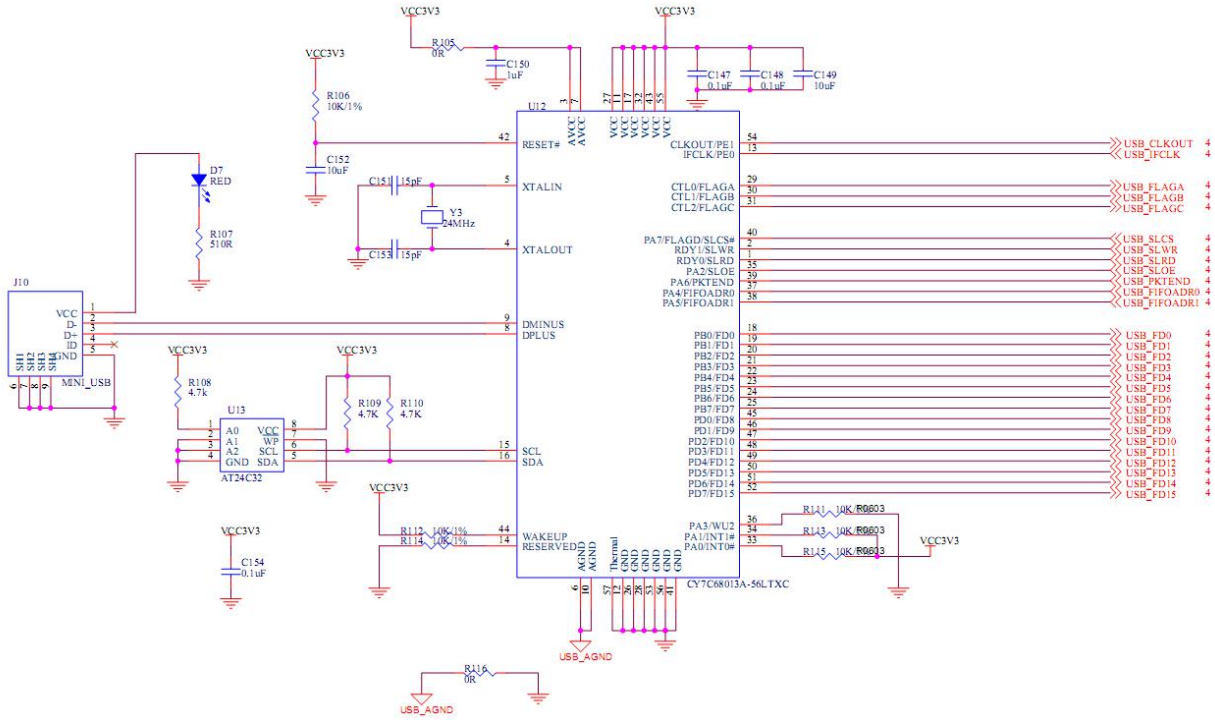

Figure 14-1: FPGA and CY7C68013A connection diagram

Figure 14-2 is a USB2.0 interface schematic, U12 is CY7C68013A, J10 is a USB interface.

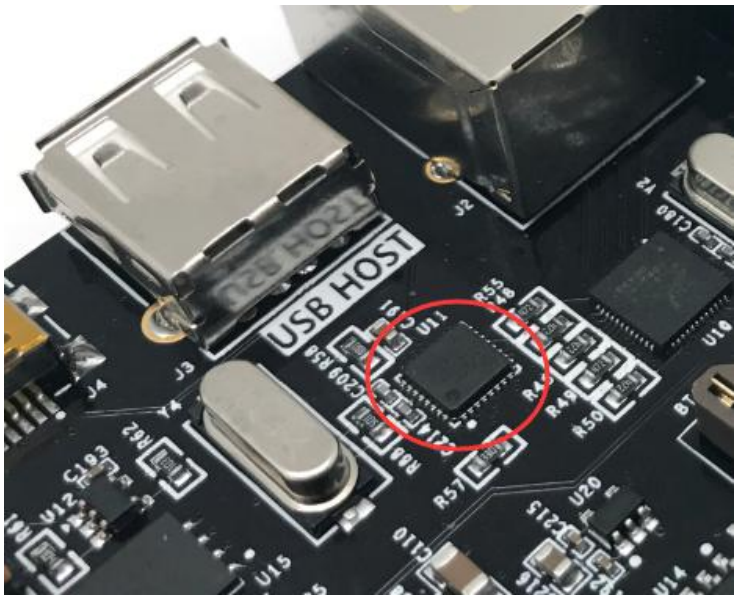

Figure 14-2: USB2.0 interface on the FPGA Board

USB2.0 Pin Assignment:

Pin Name	FPGA Pin	Description
USB_CLKOUT	K18	12-, 24- or 48 MHz clock output
USB_IFCLK	H16	Synchronous Communication Clock Signal
USB_FLAGA	F22	Status Output Signal
USB_FLAGB	F21	Status Output Signal
USB_FLAGC	G18	Status Output Signal
USB_SLCS	H20	Slave FIFO Chip Selection
USB_SLWR	K17	Slave FIF Write Signal
USB_SLRD	J17	Slave FIFO Read Signal
USB_SLOE	H18	Slave FIFO Data Output Enable
USB_PKTEND	H21	Packet End Signal
USB_FIFOADR[0]	H19	FIFO Address 0
USB_FIFOADR[1]	H22	FIFO Address 1
USB_FD[0]	C22	USB Data Bit0
USB_FD[1]	H17	USB Data Bit1
USB_FD[2]	D21	USB Data Bit2
USB_FD[3]	D22	USB Data Bit3
USB_FD[4]	E21	USB Data Bit4
USB_FD[5]	E22	USB Data Bit5
USB_FD[6]	F19	USB Data Bit6
USB_FD[7]	F20	USB Data Bit7
USB_FD[8]	J22	USB Data Bit8
USB_FD[9]	J21	USB Data Bit9
USB_FD[10]	J18	USB Data Bit10
USB_FD[11]	K22	USB Data Bit11
USB_FD[12]	K21	USB Data Bit12
USB_FD[13]	K19	USB Data Bit13
USB_FD[14]	L22	USB Data Bit14
USB_FD[15]	L21	USB Data Bit15

Part 15: Audio Interface

The AX530 FPGA development board uses the Wolfon WM8731 audio codec (CODEC) chip to provide users with a high-quality audio interface. The chip supports microphone input, line input and line output port, and the sampling rate is adjustable from 8kHz to 96kHz. The WM8731 supports audio interfaces such as I2S/PCM/AC97 and I2C control interface. Users can configure the WM8731 through the I2C bus.

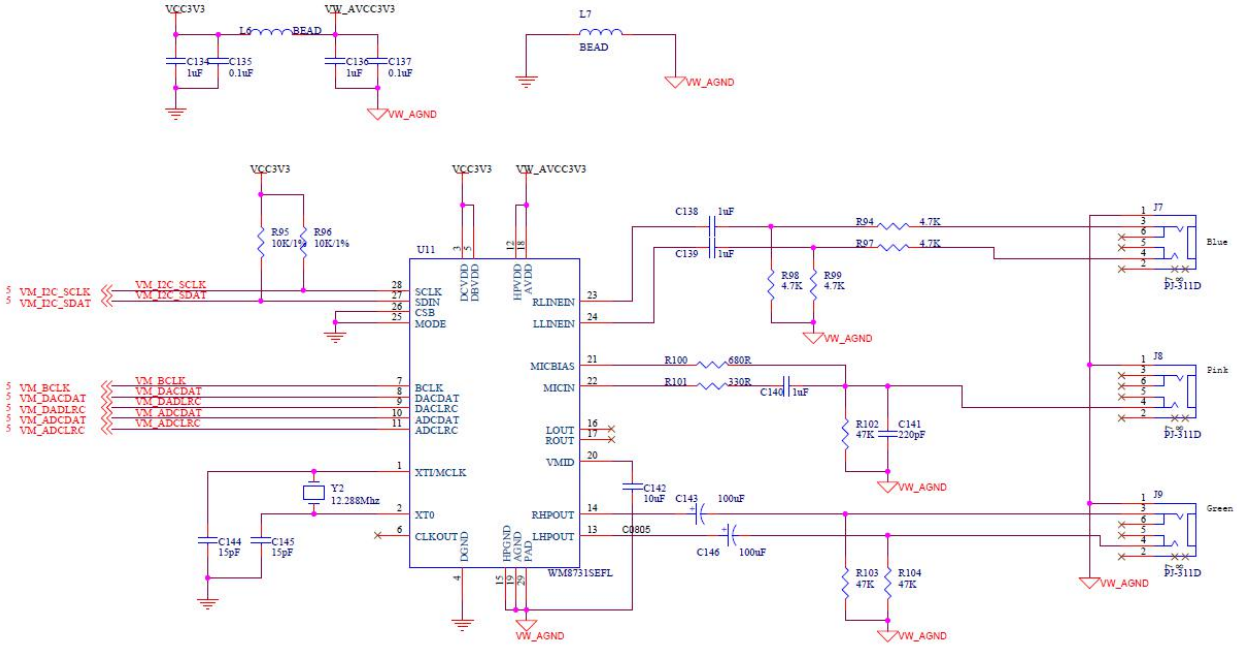

Figure 15-1: FPGA and WM8731 connection diagram

Figure 15-2 detailed the audio part on the FPGA board, U11 is WM8731 chip, J7 is the audio input, J8 is the microphone input, and J9 is the audio output.

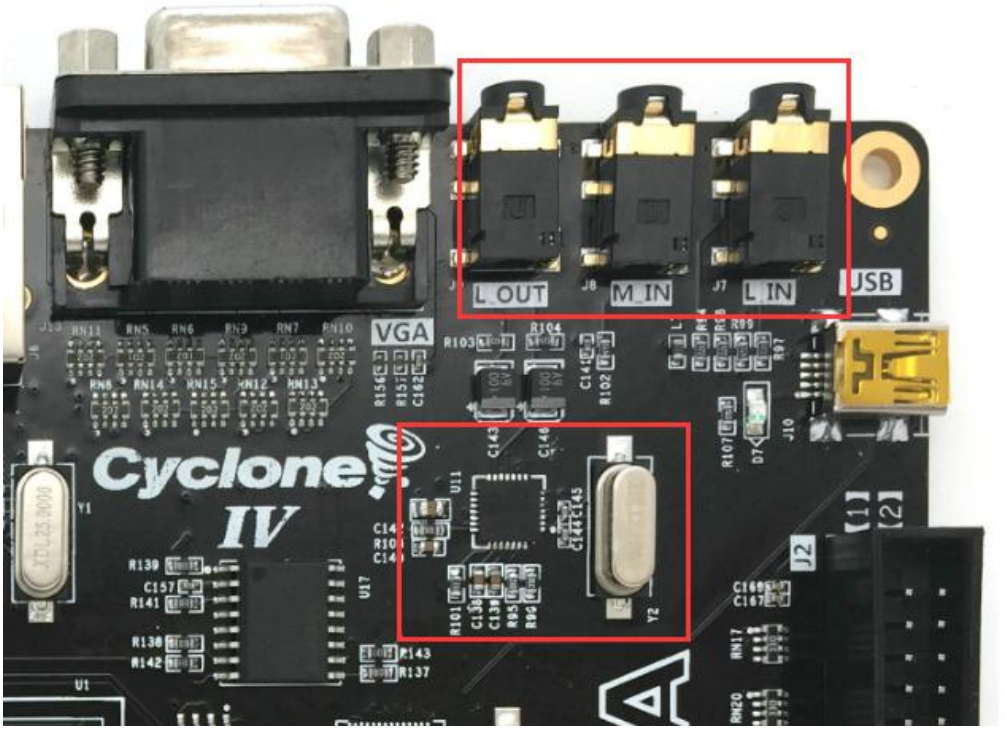

Figure 15-2: Audio interface on the FPGA board

Audio WM8731 Pin Assignment:

Pin Name	FPGA Pin	Description
VM_I2C_SCLK	A10	WM8731 IIC Clock
VM_I2C_SDAT	B10	WM8731 IIC Clock
VM_BCLK	B9	Audio data clock signal
VM_DACDAT	E10	Audio data output
VM_DACLRC	A9	Left and right channels of DAC
VM_ADCDAT	D10	Audio Data Input
VM_ADCLRC	C10	Left and right channels of DAX

Part 16: SD Card Slot

The SD card (Secure Digital Memory Card) is a memory card based on the semiconductor flash memory process. It was completed in 1999 by the Japanese Panasonic-led concept, and the participants Toshiba and SanDisk of

the United States conducted substantial research and development. In 2000, these companies initiated the establishment of the SD Association (Secure Digital Association, SDA), which has a strong lineup and attracted a large number of manufacturers. These include IBM, Microsoft, Motorola, NEC, Samsung, and others. Driven by these leading manufacturers, SD cards have become the most widely used memory card in consumer digital devices.

The SD card is a very common storage device. The SD card we have expanded supports SPI mode and SD mode. The SD card used is a MicroSD card, the schematic detailed as Figure 16-1:

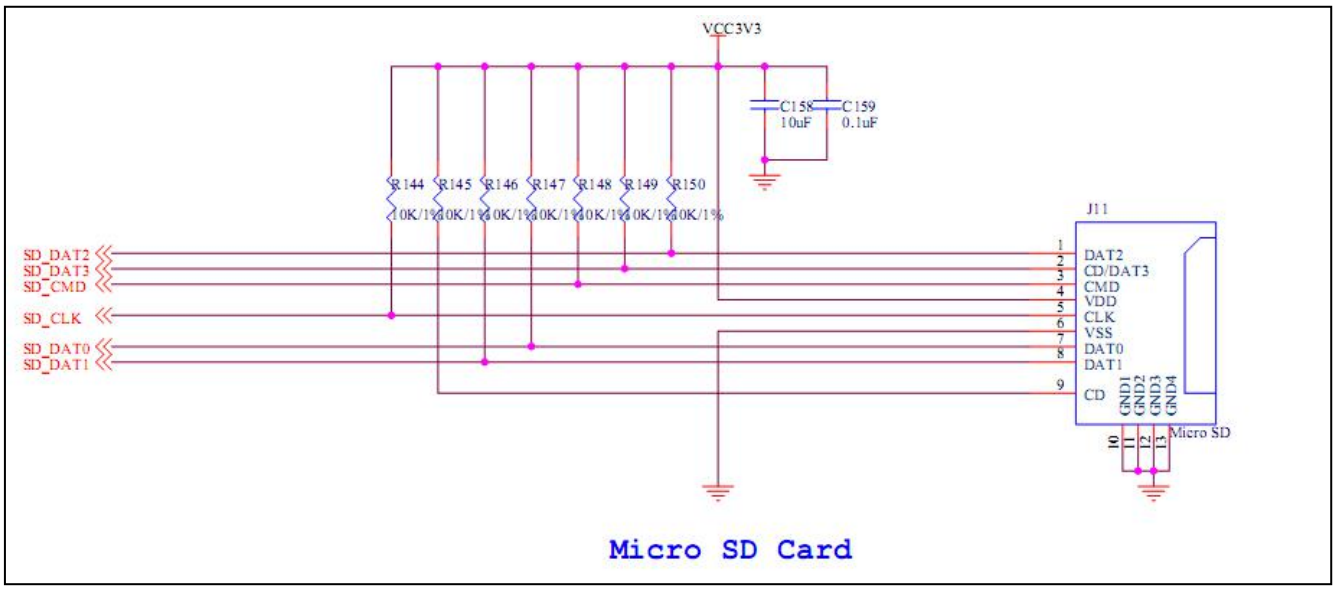

Figure 16-1: SD Card Schematic

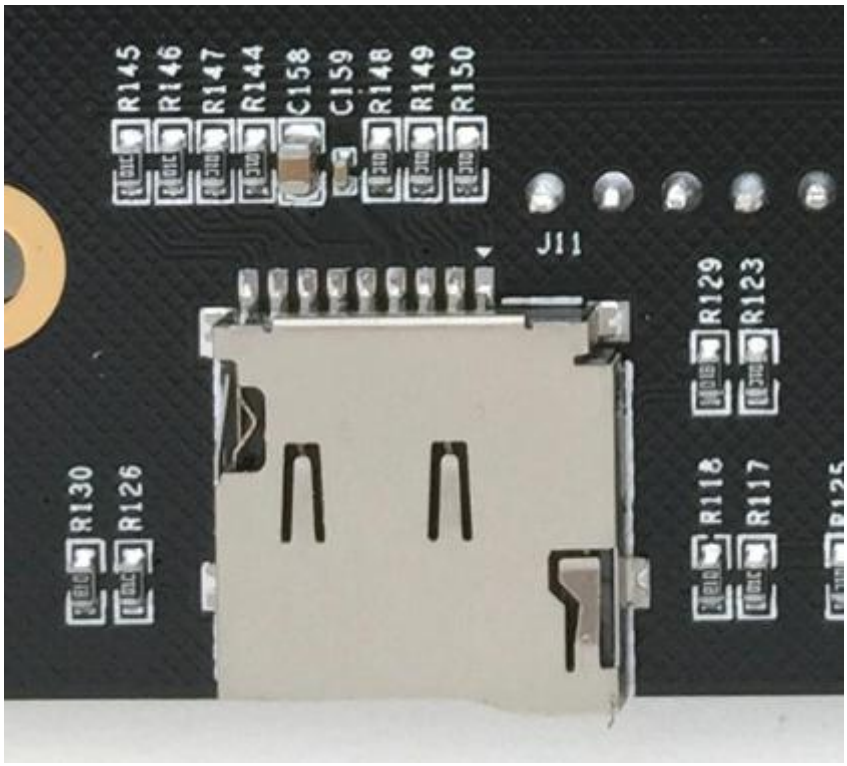

Figure 16-2: SD Cart Slot on AX515 FPGA Board

SD Card Slot Pin Assignment

SD Mode	
Pin name	FPGA Pin
SD_CLK	D20
SD_CMD	B21
SD_DAT0	C20
SD_DAT1	F17
SD_DAT2	B22
SD_DAT3	C21

Part 17: Expansion Header

The AX530 FPGA development board is reserved with three 0.1inch spacing standard 40-pin expansion headers J1, J2, J3. Each expansion header has 40 signals, of which 1-channel 5V power supply, 2-channel3.3 V power

supply, 3-channle ground and 34 IOs. **Do not directly connect the IO directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.**

A 33 ohm resistor is connected in series between the expansion port and the FPGA connection to protect the FPGA from external voltage or current. Here is a description of the connections and signals for each expansion header

Part 17.1: Expansion header J1

Figure 17-1 shows the J1 expansion port connection diagram. Pin1, Pin37, Pin38 are GND, Pin2 is +5V, and Pin39 and Pin40 are +3.3V.

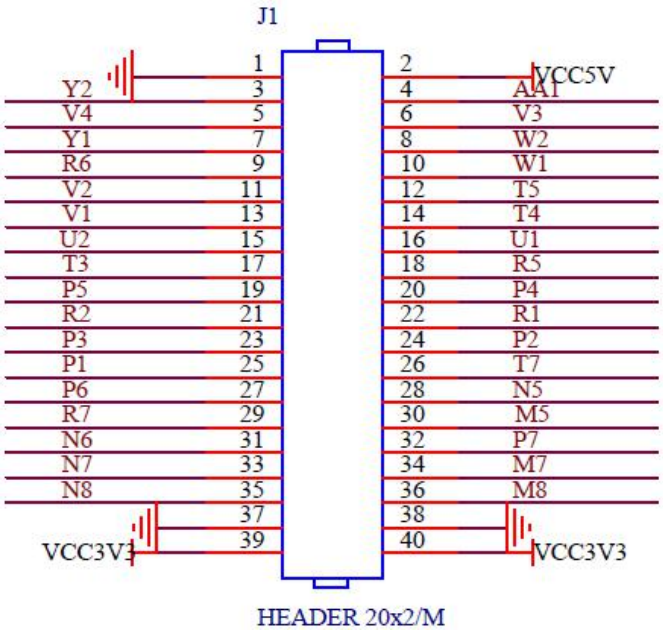

Figure 17-1: Expansion header J1 schematic

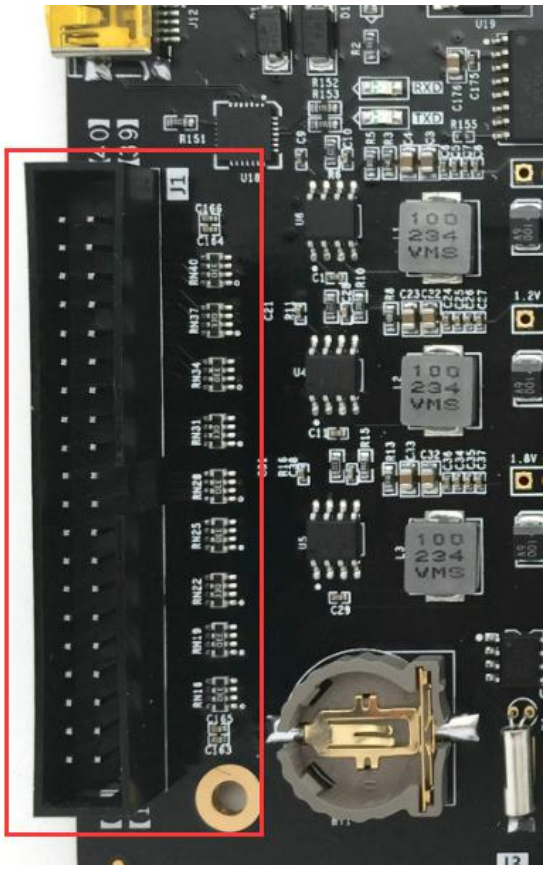

Figure 17-2: Expansion header J1 on the FPGA Board

J1 Expansion Header Pin Assignment

Pin Number	FPGA Pin	Pin Number	FPGA Pin
1	GND	**2**	VCC5V
3	Y2	**4**	AA1
5	V4	**6**	V3
7	Y1	**8**	W2
9	R6	**10**	W1
11	V2	**12**	T5
13	V1	**14**	T4
15	U2	**16**	U1
17	T3	**18**	R5
19	P5	**20**	P4
21	R2	**22**	R1

23	P3	**24**	P2
25	P1	**26**	T7
27	P6	**28**	N5
29	R7	**30**	M5
31	N6	**32**	P7
33	N7	**34**	M7
35	N8	**36**	M8
37	GND	**38**	GND
39	VCC3V3	**40**	VCC3V3

Part 17.2: Expansion header J2

Figure 17-3 shows the J1 expansion port connection diagram. Pin1, Pin37, Pin38 are GND, Pin2 is +5V, and Pin39 and Pin40 are +3.3V.

Figure 17-3 shows the J2 expansion port connection diagram. Pin1, Pin37, Pin38 are GND, Pin2 is +5V, and Pin39 and Pin40 are +3.3V. In addition to Pin33 and Pin34, the signals of J2 are connected to the Bank7 of the FPGA in differential pairs. Users can realize the data communication between LVDS2.5 and LVDS3.3

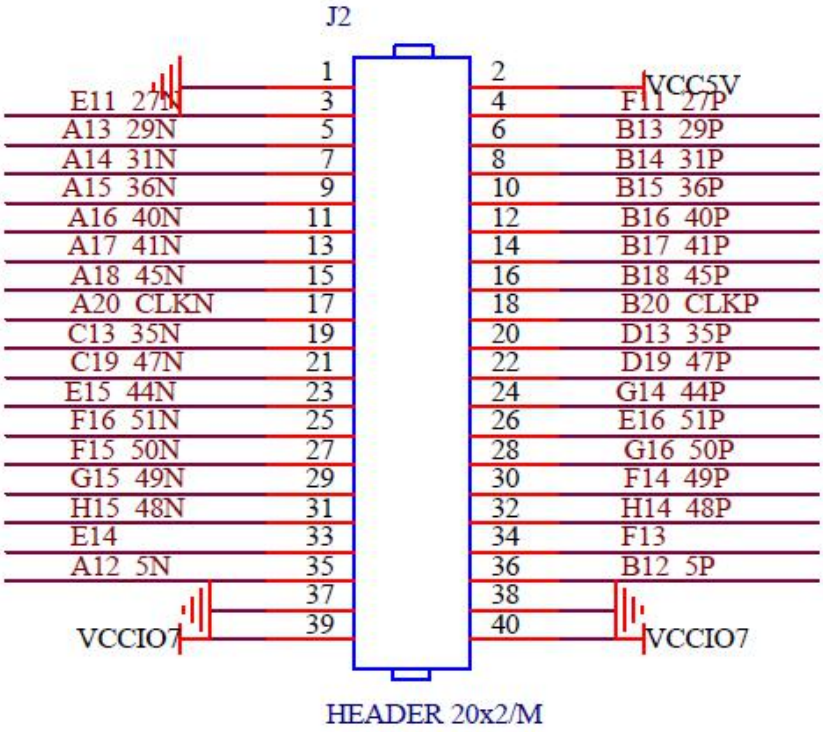

Figure 17-3: Expansion header J2 schematic

Figure 17-4 shows the differential trace of the J2 expansion port PCB. The differential line implements strict isometric, equidistant and impedance 100 ohm control.

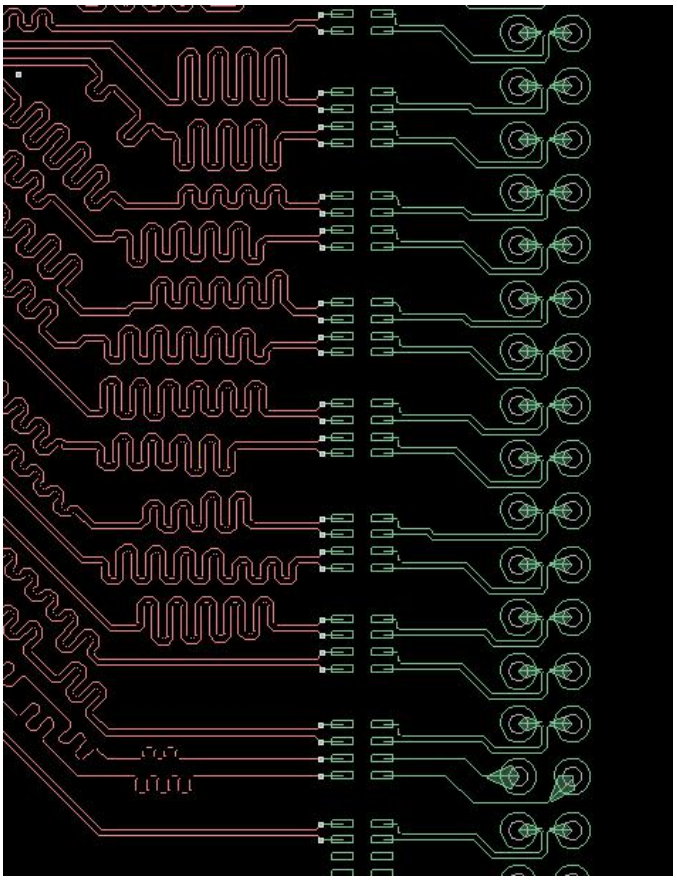

Figure 17-4: J2 expansion port PCB trace

The IO port of the J2 expansion port is connected FPGA Bank7, and the default level is 3.3V. If the user needs to modify IO of J2 to 2.5V level, you can adjust the 0 ohm resistor on the board (R158 is not installed, R159 is installed). If the user needs 1.8V IO level, the LDO (U19) power chip can be replaced by 1117-1.8.

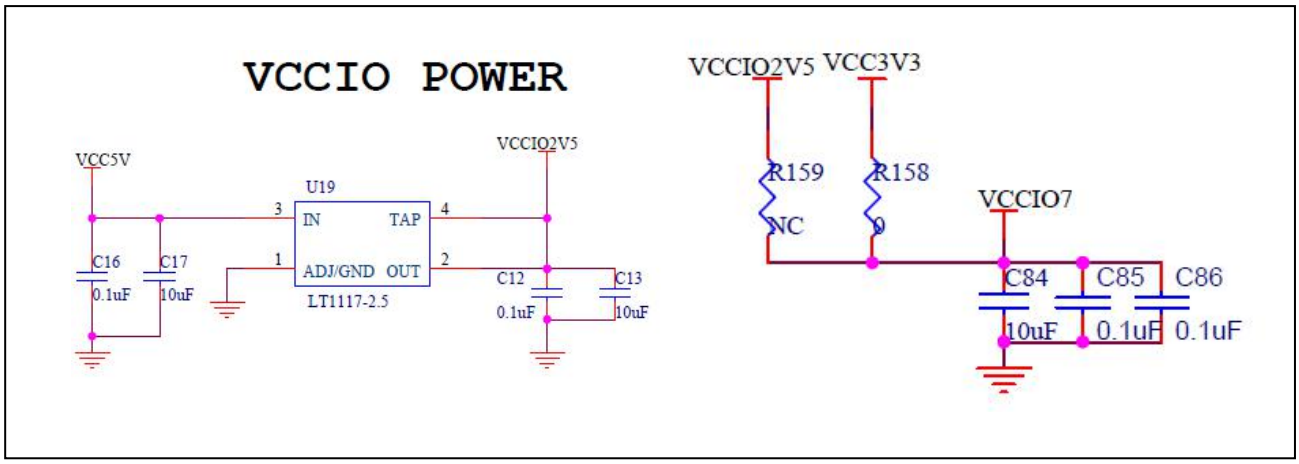

Figure 17-5: Power supply of J2 expansion port

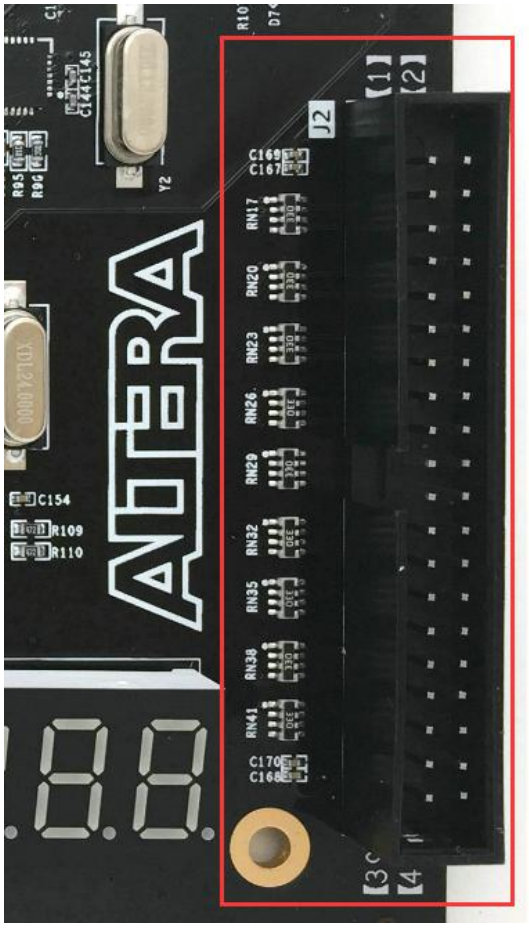

Figure 17-6: J2 expansion port on the FPGA Board

J2 Expansion Header Pin Assignment

Pin Number	FPGA Pin	Pin Number	FPGA Pin
1	GND	**2**	VCC5V
3	E11	**4**	F11
5	A13	**6**	B13
7	A14	**8**	B14
9	A15	**10**	B15
11	A16	**12**	B16
13	A17	**14**	B17
15	A18	**16**	B18
17	A20	**18**	B20
19	C13	**20**	D13
21	C19	**22**	D19
23	E15	**24**	G14
25	F16	**26**	E16
27	F15	**28**	G16
29	G15	**30**	F14
31	H15	**32**	H14
33	E14	**34**	F13
35	A12	**36**	B12
37	GND	**38**	GND
39	VCC3V3	**40**	VCC3V3

Part 17.3: Expansion header J3

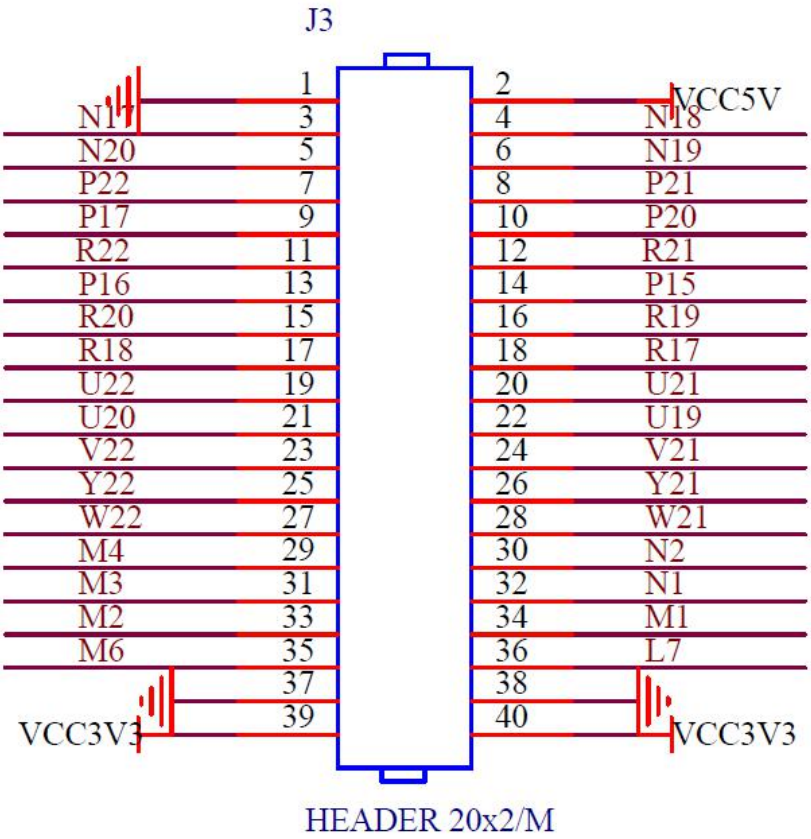

Figure 17-7: Expansion header J3 schematic

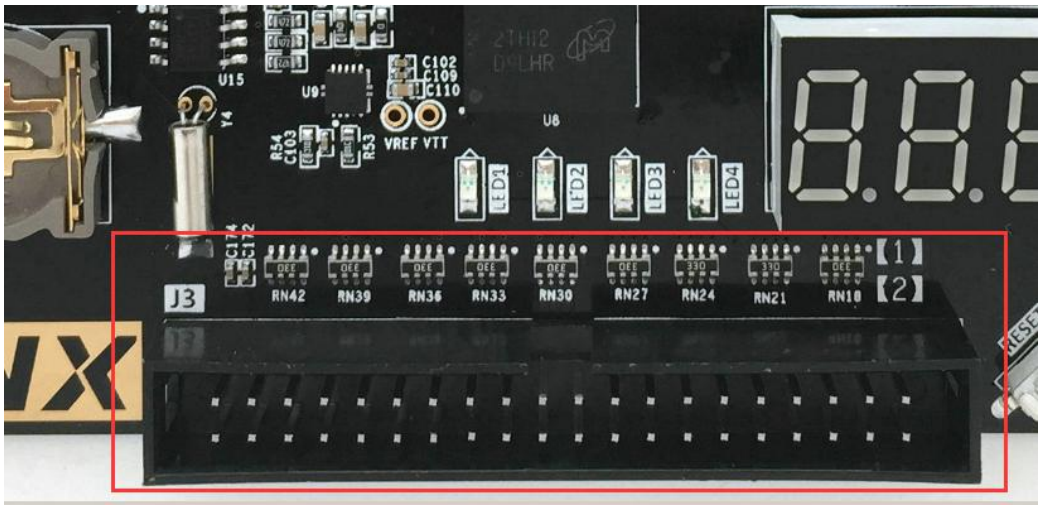

Figure 17-8: Expansion header J3 on the FPGA Board

Pin Name	FPGA Pin	Pin Name	FPGA Pin
1	GND	**2**	VCC5V
3	N17	**4**	N18
5	N20	**6**	N19
7	P22	**8**	P21
9	P17	**10**	P20
11	R22	**12**	R21
13	P16	**14**	P15
15	R20	**16**	R19
17	R18	**18**	R17
19	U22	**20**	U21
21	U20	**22**	U19
23	V22	**24**	V21
25	Y22	**26**	Y21
27	W22	**28**	W21
29	M4	**30**	N2
31	M3	**32**	N1
33	M2	**34**	M1
35	M6	**36**	L7
37	GND	**38**	GND
39	VCC3V3	**40**	VCC3V3

Part 18: LED

There are six red LEDs on the AX530 FPGA development board, one of which is the power indicator (PWR), four are users LED lights (LED1~LED4). The schematic of the four user LED sections is shown in Figure 18-1. When the FPGA pin output is logic 0, the LED will go out. When the output is logic 1, the LED is illuminated.

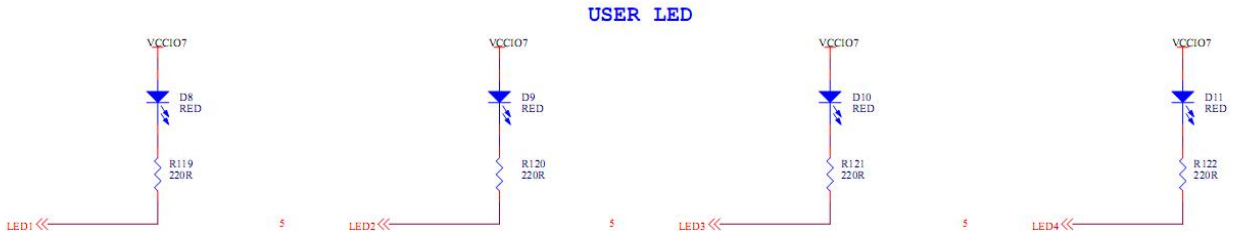

Figure 18-1: User LEDs Schematic

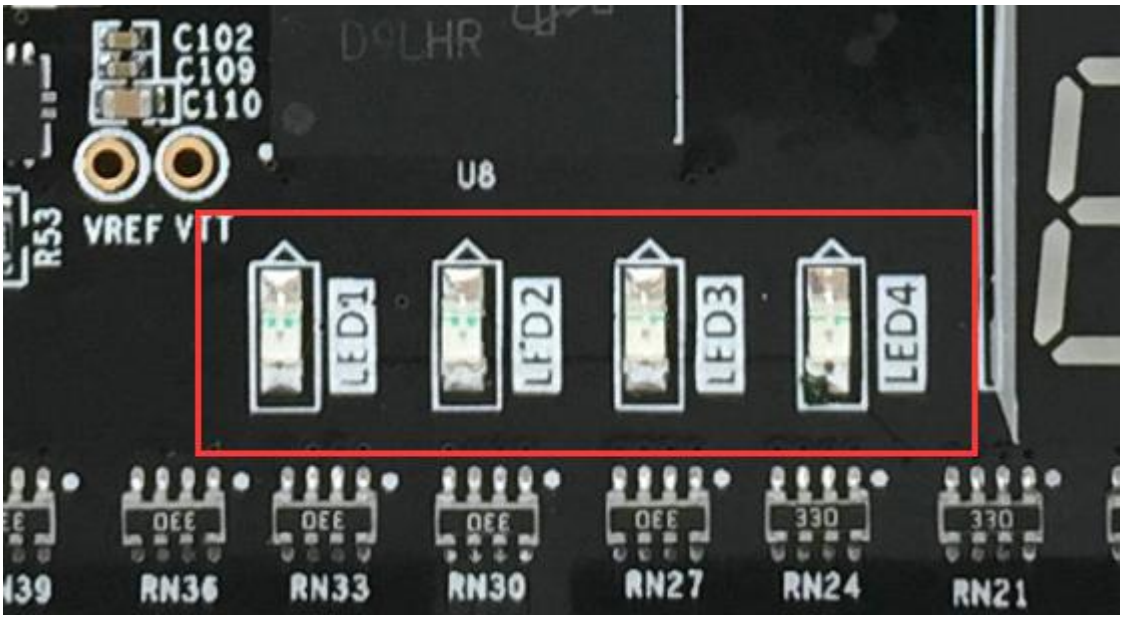

Figure 18-2: User LEDs on the FPGA Board

User LEDs Pin Assignment:

Pin Name	FPGA Pin
LED1	D15
LED2	G13
LED3	C15
LED4	E12

Part 19: Buttons

The AX530 FPGA development board has five independent buttons,

including four user buttons (KEY1~KEY4) and one reset button RESET. The buttons are active low, and the schematic diagram of the four user buttons is shown in Figure 19-1

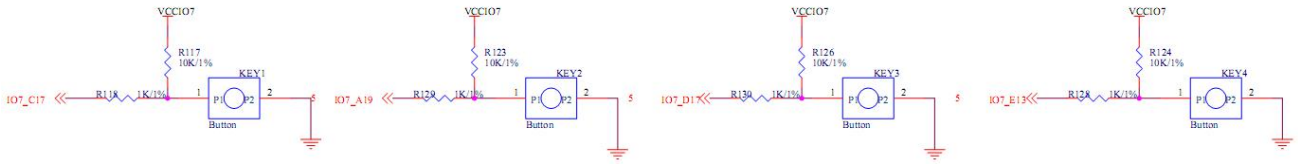

Figure 19-1: Four User Button Schematic

The reset button is connected to the normal IO of FPGA for reset FPGA program.

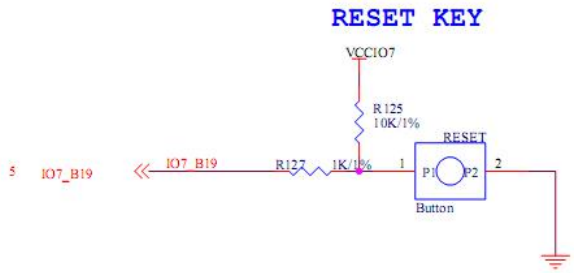

Figure 19-2: Reset Button Schematic

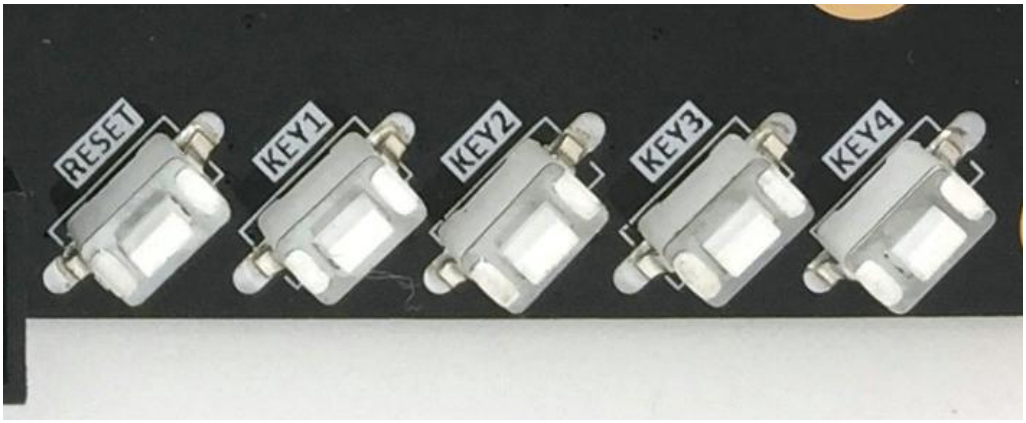

Figure 19-3: Five independent buttons on the FPGA board

Buttons Pin Assignment

Button Name	FPGA Pin	Key name
KEY1	C17	KEY 1
KEY2	A19	KEY 2
KEY3	D17	KEY 3
KEY4	E13	KEY 4
RESET	B19	RESET

Part 20: 7-segment displays

The digital tube is a very common display device. It is generally divided into a seven-segment digital tube and an eight-segment digital tube. The difference between the two is that the eight-segment digital tube has a more "point" than the seven-segment digital tube. The digital tube we use is a 6-in-one eight-segment digital tube. The segment structure of the digital tube is shown in Figure 20-1.

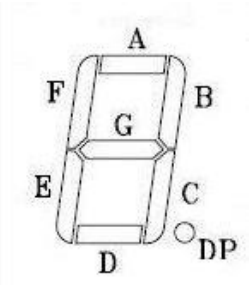

Figure 20-1: Segment Structure of Digital Tube

The AX515 FPGA development board used a common anode digital tube. **When the corresponding pin of a field is low, the corresponding field is lit. When the corresponding pin of a certain field is high, the corresponding field is not lit.**

After the above schematic, let's look at the design on the FPGA development board AX530.

The six-in-one digital tube is a dynamic display. Due to the persistence of human vision and the afterglow effect of the LED, although the digital tubes are not lit at the same time, as long as the scanning speed is fast enough, the impression is a group, stable display data, no flickering.

The same segments of the six-in-one digital tube are connected together, a total of 8 pins, and then add 6 control signal pins, a total of 14 pins, as shown in Figure 20-2, where DIG[0. .7] is the corresponding digital tube A, B, C, D, E, F, G, H (ie point DP); SEL [0..5] is the six control pins of the six digital tube, is also low level is active. When the control pin is low, the corresponding digital tube has a power supply voltage, so that the digital tube can be lit. Otherwise, no matter how the segment of the digital tube changes, the corresponding digital tube cannot be lit.

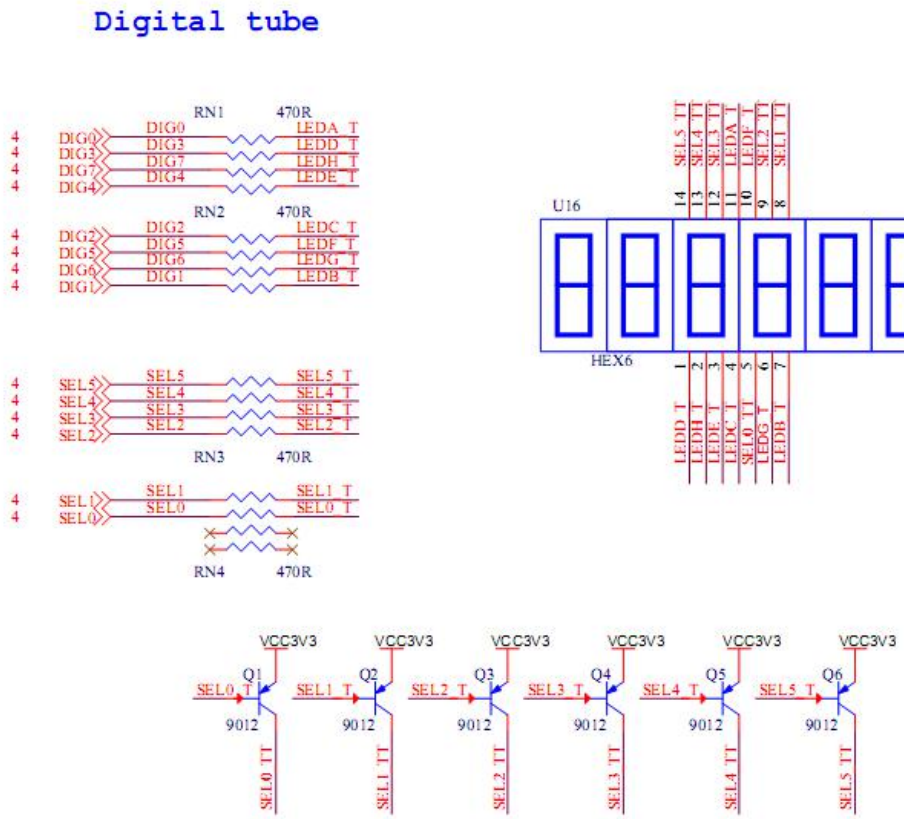

Figure 20-2: 7-segment displays Schematic

Figure 20-3: 7-segment displays on the FPGA board

7-segment displays Pin Assignments:

Pin Name	FPGA Pin	Description
SMG_Data[7]	M16	Corresponding segment DP
SMG_Data[6]	N22	Corresponding segment G
SMG_Data[5]	N21	Corresponding segment F
SMG_Data[4]	M19	Corresponding segment E
SMG_Data[3]	N16	Corresponding segment D
SMG_Data[2]	M20	Corresponding segment C
SMG_Data[1]	M22	Corresponding segment B
SMG_Data[0]	W20	Corresponding segment A
Scan_Sig[5]	W19	The first digital tube from the right
Scan_Sig[4]	AA21	The second digital tube from the right
Scan_Sig[3]	T18	The third digital tube from the right
Scan_Sig[2]	T17	The fourth digital tube from the right
Scan_Sig[1]	G17	The fifth digital tube from the right
Scan_Sig[0]	M21	The sixth digital tube from the right