ZYNQ7000 FPGA Core Board AC7Z035

User Manual

ALINX

Version Record

Version	Date	Release By	Description
Rev 1.0	2019-04-05	Rachel Zhou	First Release

Table of Contents

Version Record.....2
Part 1: AC7Z035 core board.....4
Part 1.1: AC7Z035 core board Introduction.....4
Part 1.2: ZYNQ Chip.....6
Part 1.3: DDR3 DRAM.....9
Part 1.4: QSPI Flash.....14
Part 1.5: eMMC Flash.....16
Part 1.6: Clock Configuration.....17
Part 1.7: LED Light.....20
Part 1.8: Reset circuit.....21
Part 1.9: Power Supply.....22
Part 1.10: AC7Z035 Core Board Size Dimension.....24
Part 1.11: Board to Board Connectors pin assignment.....25

Part 1: AC7Z035 core board

Part 1.1: AC7Z035 core board Introduction

AC7Z035 (core board model, the same below) FPGA core board, ZYNQ chip is based on XC7Z035-2FFG676 of XILINX company ZYNQ7000 series. The ZYNQ chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. The FPGA of the ZYNQ chip contains a wealth of programmable logic cells, DSP and internal RAM.

The core board uses four Micron 512MB DDR3 chips MT41J256M16HA-125 for a total capacity of 4GB. Two DDR3s are mounted on the PS and PL sides, respectively, which form a 32-bit bus width. The DDR3 SDRAM on the PS side can run at up to 533MHz (data rate 1066Mbps), and the DDR3 SDRAM on the PL side can run at speeds up to 800MHz (data rate 1600Mbps). In addition, two 256MBit QSPI FLASH and 8GB eMMC FLASH chips are integrated on the core board to boot the storage configuration and system files.

In order to connect with the carrier board, the four board-to-board connectors of the core board expand the USB interface, the Gigabit Ethernet interface, the SD card interface and other remaining IO ports of the PS side; and also extend the 8-pair high-speed transceiver GTX interface of the ZYNQ, almost all IO ports (144) on the PL side. The level of IO of BANK12 and BANK13 can be modified by replacing the LDO chip on the core board to meet the requirements of different level interfaces of users. For users who need a lot of IO, this core board will be a good choice. Moreover, the IO connection part, the routing between the ZYNQ chip and the interface is equal length and differential processing, and the core board size is only 80*60 (mm), which is

very suitable for secondary development.

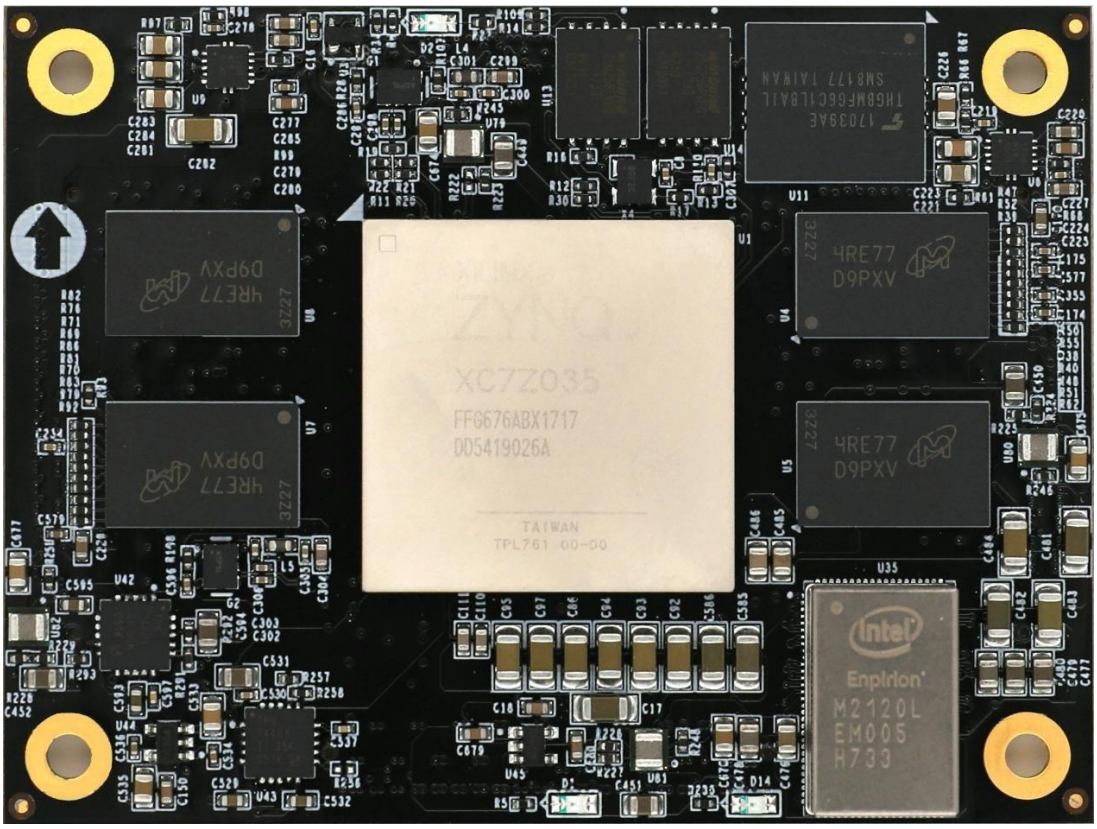

Figure 2-1-1: AC7Z035 Core Board (Front View)

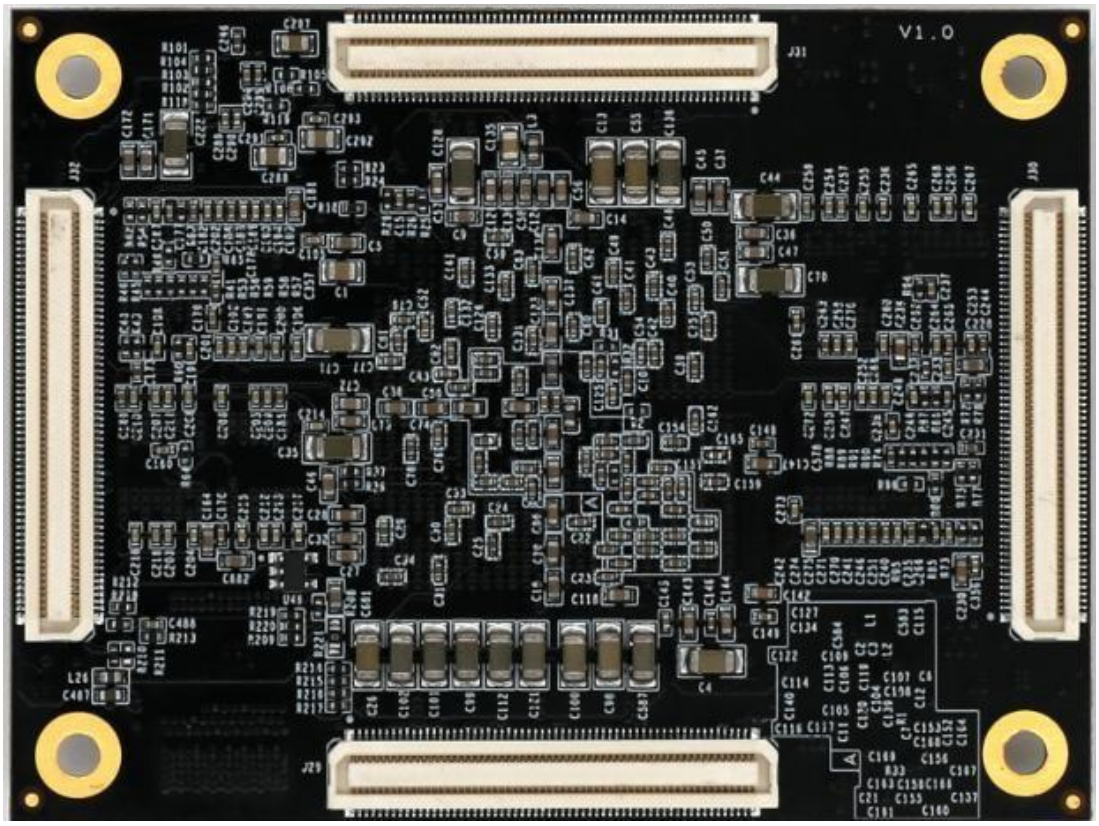

Figure 2-1-2: AC7Z035 Core Board (Rear View)

Part 1.2: ZYNQ Chip

The FPGA core board AC7Z035 uses Xilinx's Zynq7000 series chip, model XC7Z035-2FFG676. The chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO etc. The PS can operate independently and start up at power on or reset. Figure 2-2-1 detailed the Overall Block Diagram of the ZYNQ7000 Chip.

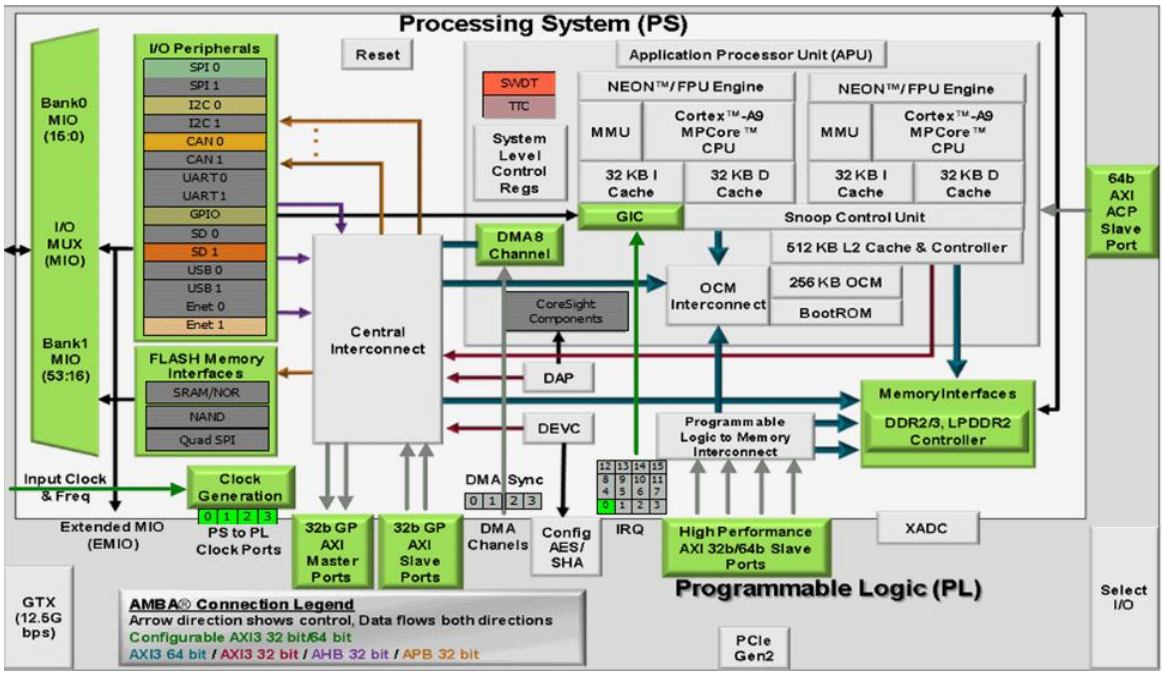

Figure 2-2-1: Overall Block Diagram of the ZYNQ7000 Chip

The main parameters of the PS system part are as follows:

- ARM dual-core CortexA9-based application processor, ARM-v7 architecture, up to 800MHz
- 32KB level 1 instruction and data cache per CPU, 512KB level 2 cache

2 CPU shares

- On-chip boot ROM and 256KB on-chip RAM
- External storage interface, support 16/32 bit DDR2, DDR3 interface
- Two Gigabit NIC support: divergent-aggregate DMA, GMII, RGMII, SGMII interface
- Two USB2.0 OTG interfaces, each supporting up to 12 nodes
- Two CAN2.0B bus interfaces
- Two SD card, SDIO, MMC compatible controllers
- 2 SPIs, 2 UARTs, 2 I2C interfaces
- 54 multi-function IOs that can be configured as normal IO or peripheral control interfaces
- High bandwidth connection within PS and PS to PL

The main parameters of the PL logic part are as follows:

- Logic Cells: 275K
- Look-up-tables (LUTs): 171,900
- Flip-flops: 343,800
- 18x25MACCs：900
- Block RAM：17.6Mb
- 8-channel high-speed GTX transceiver, supporting PCIE Gen2x8;
- Two AD converters for on-chip voltage, temperature sensing and up to 17 external differential input channels, 1MBPS

XC7Z035-2FFG676I chip speed grade is -2, industrial grade, package is FGG676, pin pitch is 1.0mm the specific chip model definition of ZYNQ7000 series is shown in Figure 2-2-2

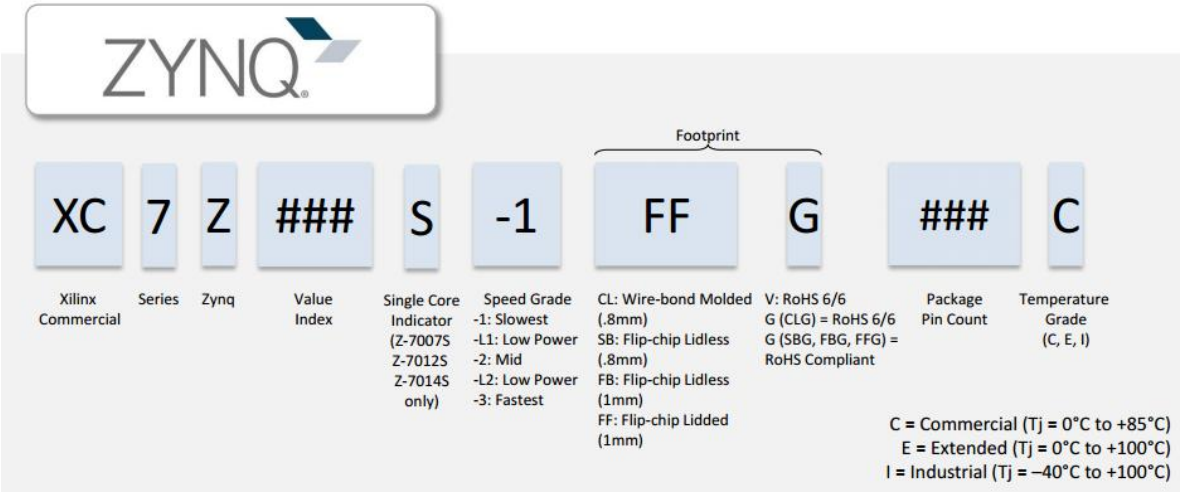

Figure 2-2-2: The Specific Chip Model Definition of ZYNQ7000 Series

Figure 2-2-3: The XC7Z035 chip used on the Core Board

Part 1.3: DDR3 DRAM

The FPGA core board AC7Z035 is equipped with four Micron 512MB DDR3 chips, model MT41J256M16HA-125 (compatible with MT41K256M16HA-125), in which Two DDR3s are mounted on the PS and PL sides respectively. Two DDR3 SDRAMs form a 32-bit bus width. The PS-side DDR3 SDRAM has a maximum operating speed of 533MHz (data rate 1066Mbps), and two DDR3 memory systems are directly connected to the memory interface of the BANK 502 of the ZYNQ Processing System (PS). The PL-side DDR3 SDRAM has a maximum operating speed of 800MHz (data rate 1600Mbps), and two DDR3 memory systems are connected to the BANK33 and BANK34 interfaces of the FPGA. The specific configuration of DDR3 SDRAM is shown in Table 2-3-1.

Bit Number	Chip Model	Capacity	Factory
U4,U5,U7,U8	MT41J256M16HA-125	256M x 16bit	Micron

Table 2-3-1: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

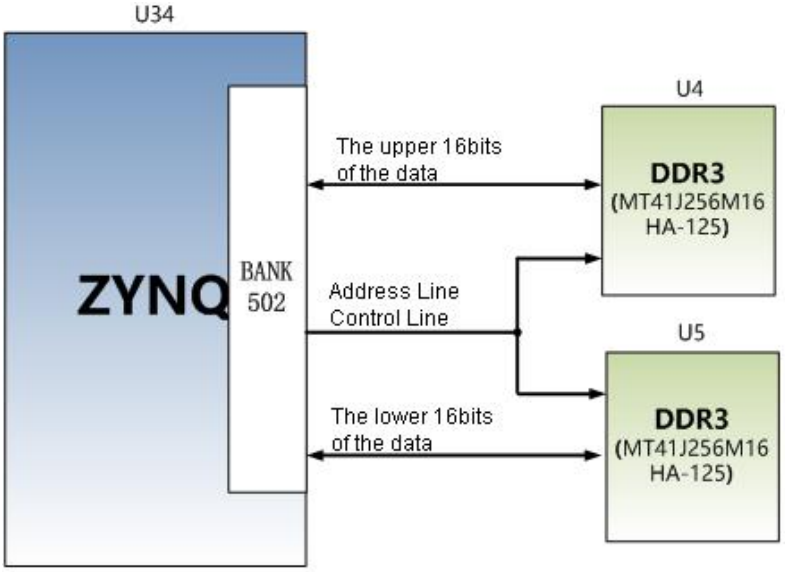

Figure 2-3-1: The Schematic Part of DDR3 DRAM on the PS side

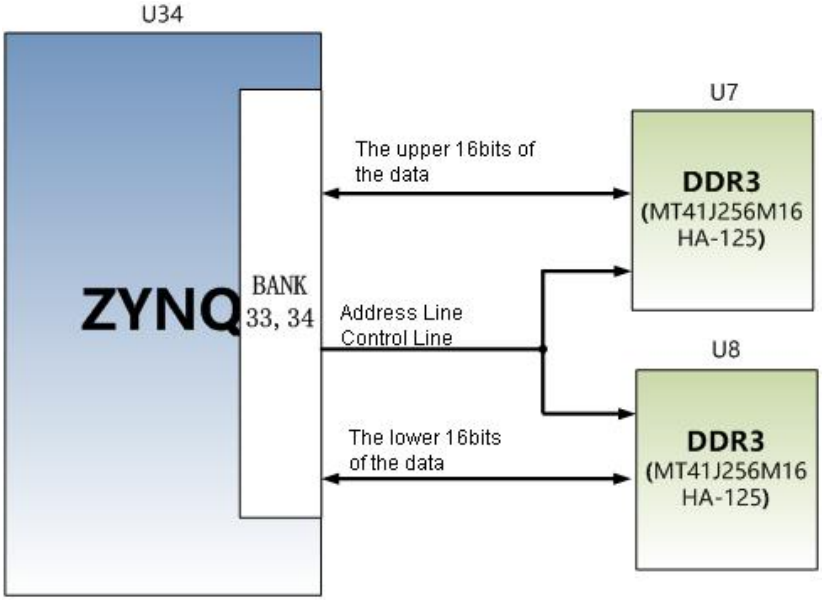

Figure 2-3-2: The Schematic Part of DDR3 DRAM on the PL side

PS side DDR3 DRAM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
PS_DDR3_DQS0_P	PS_DDR_DQS_P0_502	H24
PS_DDR3_DQS0_N	PS_DDR_DQS_N0_502	G25
PS_DDR3_DQS1_P	PS_DDR_DQS_P1_502	L24
PS_DDR3_DQS1_N	PS_DDR_DQS_N1_502	L25
PS_DDR3_DQS2_P	PS_DDR_DQS_P2_502	P25
PS_DDR3_DQS2_N	PS_DDR_DQS_N2_502	R25

PS_DDR3_DQS3_P	PS_DDR_DQS_P3_502	W24
PS_DDR3_DQS4_N	PS_DDR_DQS_N3_502	W25
PS_DDR3_D0	PS_DDR_DQ0_502	J26
PS_DDR3_D1	PS_DDR_DQ1_502	F25
PS_DDR3_D2	PS_DDR_DQ2_502	J25
PS_DDR3_D3	PS_DDR_DQ3_502	G26
PS_DDR3_D4	PS_DDR_DQ4_502	H26
PS_DDR3_D5	PS_DDR_DQ5_502	H23
PS_DDR3_D6	PS_DDR_DQ6_502	J24
PS_DDR3_D7	PS_DDR_DQ7_502	J23
PS_DDR3_D8	PS_DDR_DQ8_502	K26
PS_DDR3_D9	PS_DDR_DQ9_502	L23
PS_DDR3_D10	PS_DDR_DQ10_502	M26
PS_DDR3_D11	PS_DDR_DQ11_502	K23
PS_DDR3_D12	PS_DDR_DQ12_502	M25
PS_DDR3_D13	PS_DDR_DQ13_502	N24
PS_DDR3_D14	PS_DDR_DQ14_502	M24
PS_DDR3_D15	PS_DDR_DQ15_502	N23
PS_DDR3_D16	PS_DDR_DQ16_502	R26
PS_DDR3_D17	PS_DDR_DQ17_502	P24
PS_DDR3_D18	PS_DDR_DQ18_502	N26
PS_DDR3_D19	PS_DDR_DQ19_502	P23
PS_DDR3_D20	PS_DDR_DQ20_502	T24
PS_DDR3_D21	PS_DDR_DQ21_502	T25
PS_DDR3_D22	PS_DDR_DQ22_502	T23
PS_DDR3_D23	PS_DDR_DQ23_502	R23
PS_DDR3_D24	PS_DDR_DQ24_502	V24
PS_DDR3_D25	PS_DDR_DQ25_502	U26
PS_DDR3_D26	PS_DDR_DQ26_502	U24
PS_DDR3_D27	PS_DDR_DQ27_502	U25
PS_DDR3_D28	PS_DDR_DQ28_502	W26
PS_DDR3_D29	PS_DDR_DQ29_502	Y25
PS_DDR3_D30	PS_DDR_DQ30_502	Y26
PS_DDR3_D31	PS_DDR_DQ31_502	W23
PS_DDR3_DM0	PS_DDR_DM0_502	G24
PS_DDR3_DM1	PS_DDR_DM1_502	K25

PS_DDR3_DM2	PS_DDR_DM2_502	P26
PS_DDR3_DM3	PS_DDR_DM3_502	V26
PS_DDR3_A0	PS_DDR_A0_502	K22
PS_DDR3_A1	PS_DDR_A1_502	K20
PS_DDR3_A2	PS_DDR_A2_502	N21
PS_DDR3_A3	PS_DDR_A3_502	L22
PS_DDR3_A4	PS_DDR_A4_502	M20
PS_DDR3_A5	PS_DDR_A5_502	N22
PS_DDR3_A6	PS_DDR_A6_502	L20
PS_DDR3_A7	PS_DDR_A7_502	J21
PS_DDR3_A8	PS_DDR_A8_502	T20
PS_DDR3_A9	PS_DDR_A9_502	U20
PS_DDR3_A10	PS_DDR_A10_502	M22
PS_DDR3_A11	PS_DDR_A11_502	H21
PS_DDR3_A12	PS_DDR_A12_502	P20
PS_DDR3_A13	PS_DDR_A13_502	J20
PS_DDR3_A14	PS_DDR_A14_502	R20
PS_DDR3_BA0	PS_DDR_BA0_502	U22
PS_DDR3_BA1	PS_DDR_BA1_502	T22
PS_DDR3_BA2	PS_DDR_BA2_502	R22
PS_DDR3_S0	PS_DDR_CS_B_502	Y21
PS_DDR3_RAS	PS_DDR_RAS_B_502	V23
PS_DDR3_CAS	PS_DDR_CAS_B_502	Y23
PS_DDR3_WE	PS_DDR_WE_B_502	V22
PS_DDR3_ODT	PS_DDR_ODT_502	Y22
PS_DDR3_RESET	PS_DDR_DRST_B_502	H22
PS_DDR3_CLK0_P	PS_DDR_CKP_502	R21
PS_DDR3_CLK0_N	PS_DDR_CKN_502	P21
PS_DDR3_CKE	PS_DDR_CKE_502	U21

PL side DDR3 DRAM pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
PL_DDR3_DQS0_P	IO_L3P_T0_DQS_33	G2
PL_DDR3_DQS0_N	IO_L3N_T0_DQS_33	F2
PL_DDR3_DQS1_P	IO_L9P_T1_DQS_33	K2

PL_DDR3_DQS1_N	IO_L9N_T1_DQS_33	K1
PL_DDR3_DQS2_P	IO_L15P_T2_DQS_33	N3
PL_DDR3_DQS2_N	IO_L15N_T2_DQS_33	N2
PL_DDR3_DQS3_P	IO_L21P_T3_DQS_33	M8
PL_DDR3_DQS4_N	IO_L21N_T3_DQS_33	L8
PL_DDR3_D0	IO_L5N_T0_33	E1
PL_DDR3_D1	IO_L1N_T0_33	F4
PL_DDR3_D2	IO_L4P_T0_33	D1
PL_DDR3_D3	IO_L1P_T0_33	G4
PL_DDR3_D4	IO_L2N_T0_33	D3
PL_DDR3_D5	IO_L5P_T0_33	E2
PL_DDR3_D6	IO_L2P_T0_33	D4
PL_DDR3_D7	IO_L4N_T0_33	C1
PL_DDR3_D8	IO_L7N_T1_33	H1
PL_DDR3_D9	IO_L10N_T1_33	G1
PL_DDR3_D10	IO_L7P_T1_33	J1
PL_DDR3_D11	IO_L8N_T1_33	H3
PL_DDR3_D12	IO_L11N_T1_SRCC_33	K3
PL_DDR3_D13	IO_L8P_T1_33	H4
PL_DDR3_D14	IO_L11P_T1_SRCC_33	L3
PL_DDR3_D15	IO_L10P_T1_33	H2
PL_DDR3_D16	IO_L18P_T2_33	N1
PL_DDR3_D17	IO_L14P_T2_SRCC_33	L5
PL_DDR3_D18	IO_L14N_T2_SRCC_33	L4
PL_DDR3_D19	IO_L13P_T2_MRCC_33	M6
PL_DDR3_D20	IO_L16P_T2_33	M2
PL_DDR3_D21	IO_L17P_T2_33	N4
PL_DDR3_D22	IO_L16N_T2_33	L2
PL_DDR3_D23	IO_L17N_T2_33	M4
PL_DDR3_D24	IO_L23P_T3_33	N7
PL_DDR3_D25	IO_L22N_T3_33	J6
PL_DDR3_D26	IO_L19P_T3_33	M7
PL_DDR3_D27	IO_L20N_T3_33	J5
PL_DDR3_D28	IO_L24P_T3_33	K8
PL_DDR3_D29	IO_L20P_T3_33	K5
PL_DDR3_D30	IO_L24N_T3_33	K7

PL_DDR3_D31	IO_L22P_T3_33	K6
PL_DDR3_DM0	IO_L6P_T0_33	F3
PL_DDR3_DM1	IO_L12P_T1_MRCC_33	J4
PL_DDR3_DM2	IO_L13N_T2_MRCC_33	M5
PL_DDR3_DM3	IO_L23N_T3_33	N6
PL_DDR3_A0	IO_L17N_T2_34	A8
PL_DDR3_A1	IO_L23P_T3_34	C2
PL_DDR3_A2	IO_L14P_T2_SRCC_34	D6
PL_DDR3_A3	IO_L15N_T2_DQS_34	B9
PL_DDR3_A4	IO_L10N_T1_34	D5
PL_DDR3_A5	IO_L17P_T2_34	A9
PL_DDR3_A6	IO_L11N_T1_SRCC_34	E7
PL_DDR3_A7	IO_L15P_T2_DQS_34	C9
PL_DDR3_A8	IO_L12N_T1_MRCC_34	F7
PL_DDR3_A9	IO_L18N_T2_34	A7
PL_DDR3_A10	IO_L24N_T3_34	A2
PL_DDR3_A11	IO_L11P_T1_SRCC_34	F8
PL_DDR3_A12	IO_L23N_T3_34	B1
PL_DDR3_A13	IO_L16P_T2_34	B10
PL_DDR3_A14	IO_L12P_T1_MRCC_34	G7
PL_DDR3_BA0	IO_L18P_T2_34	B7
PL_DDR3_BA1	IO_L19N_T3_VREF_34	C3
PL_DDR3_BA2	IO_L22N_T3_34	A3
PL_DDR3_S0	IO_L14N_T2_SRCC_34	C6
PL_DDR3_RAS	IO_L19P_T3_34	C4
PL_DDR3_CAS	IO_L20N_T3_34	B4
PL_DDR3_WE	IO_L20P_T3_34	B5
PL_DDR3_ODT	IO_L22P_T3_34	A4
PL_DDR3_RESET	IO_L16N_T2_34	A10
PL_DDR3_CLK0_P	IO_L21P_T3_DQS_34	B6
PL_DDR3_CLK0_N	IO_L21N_T3_DQS_34	A5
PL_DDR3_CKE	IO_L24P_T3_34	B2

Part 1.4: QSPI Flash

The FPGA core board AC7Z035 is equipped with two 256MBit Quad-SPI FLASH chips to form an 8-bit bandwidth data bus, the flash model is

W25Q256FVEI, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 2-4-1.

Position	Model	Capacity	Factory
U13,U14	W25Q256FVEI	256M bit	Winbond

Table 2-4-1: QSPI FLASH Specification

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 2-4-1 shows the QSPI Flash in the schematic.

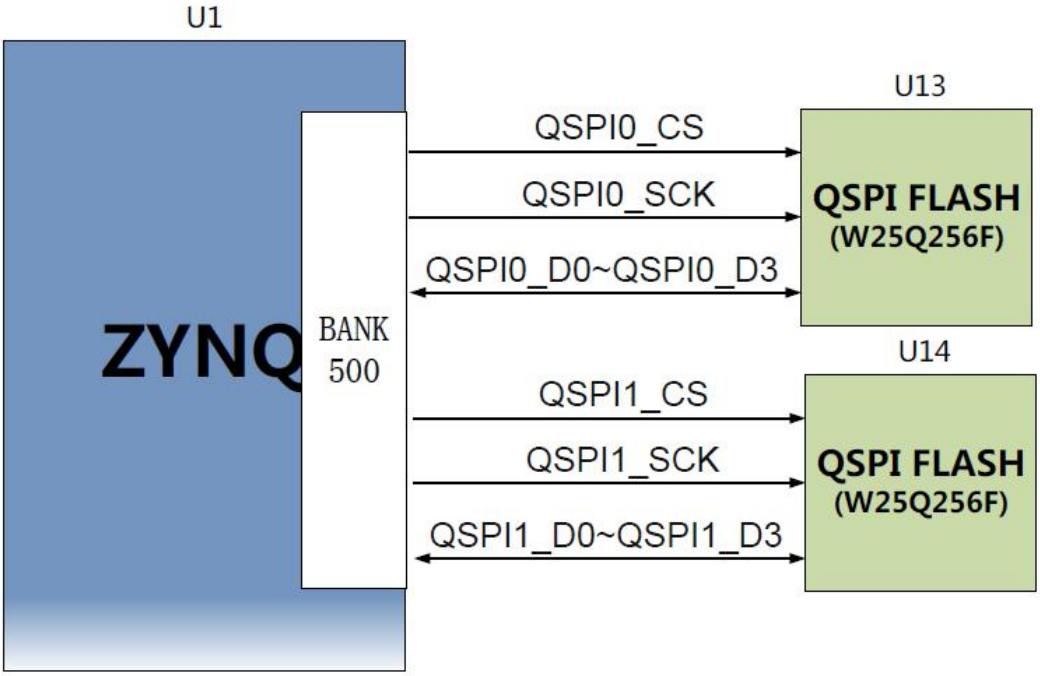

Figure 2-4-1: QSPI Flash in the schematic

Configure chip pin assignments:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
QSPI0_SCK	PS_MIO6_500	F23

QSPI0_CS	PS_MIO1_500	D26
QSPI0_D0	PS_MIO2_500	E25
QSPI0_D1	PS_MIO3_500	D25
QSPI0_D2	PS_MIO4_500	F24
QSPI0_D3	PS_MIO5_500	C26
QSPI1_SCK	PS_MIO9_500	D24
QSPI1_CS	PS_MIO0_500	E26
QSPI1_D0	PS_MIO10_500	A25
QSPI1_D1	PS_MIO11_500	B26
QSPI1_D2	PS_MIO12_500	A23
QSPI1_D3	PS_MIO13_500	B25

Part 1.5: eMMC Flash

The FPGA core board AC7Z035 is equipped with a large-capacity 8GB eMMC FLASH chip, model THGBMFG6C1LBAIL, which supports the JEDEC e-MMC V5.0 standard HS-MMC interface with level support of 1.8V or 3.3V. The data width of the eMMC FLASH and ZYNQ connections is 4 bits. Due to the large capacity and non-volatile nature of eMMC FLASH, it can be used as a large-capacity storage device for the ZYNQ system, such as ARM applications, system files and other user data files. The specific models and related parameters of eMMC FLASH are shown in Table2-5-1.

Position	Model	Capacity	Factory
U11	THGBMFG6C1LBAIL	8G Byte	TOSHIBA

Table2-5-1: eMMC FLASH Specification

eMMC FLASH is connected to the GPIO port of the BANK501 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the SD interface. Figure 2-5-1 shows the eMMC Flash in the schematic.

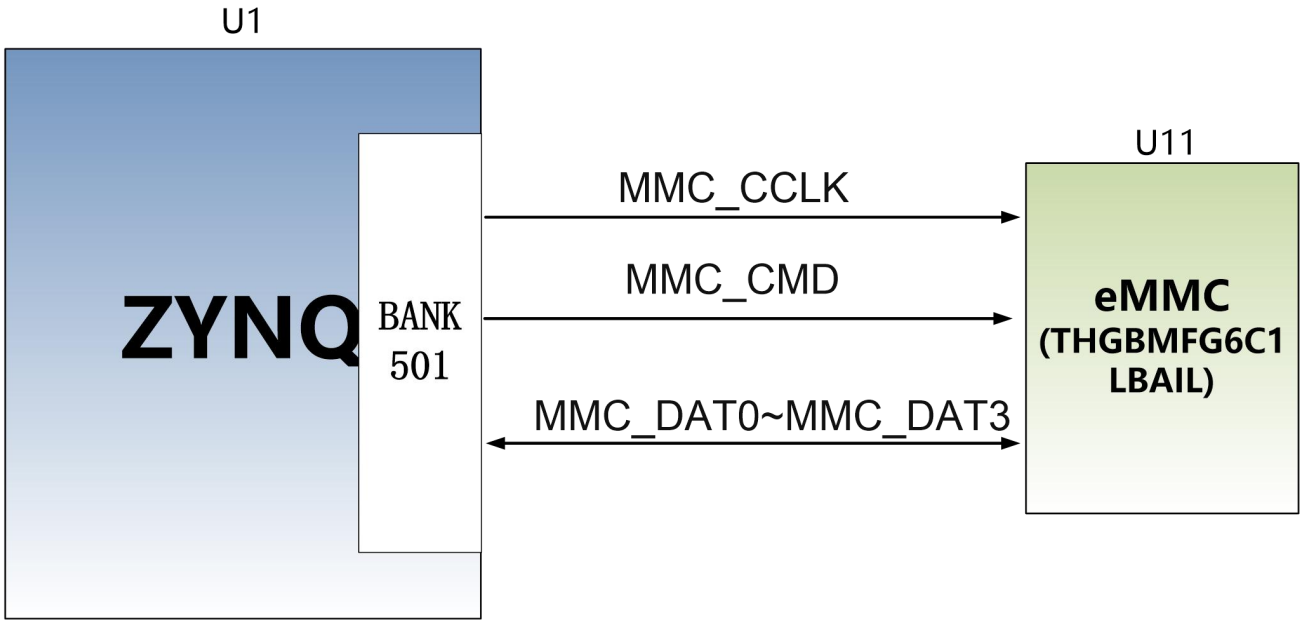

Figure 2-5-1: eMMC Flash in the Schematic

Pin Assignment of eMMC Flash

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
MMC_CCLK	PS_MIO48_501	B21
MMC_CMD	PS_MIO47_501	B19
MMC_D0	PS_MIO46_501	E17
MMC_D1	PS_MIO49_501	A18
MMC_D2	PS_MIO50_501	B22
MMC_D3	PS_MIO51_501	B20

Part 1.6: Clock Configuration

The core system provides a reference clock for the PS system, the PL logic section, and the GTX transceiver, allowing the PS system and PL logic to work independently. The schematic diagram of the clock circuit design is shown in Figure 2-6-1:

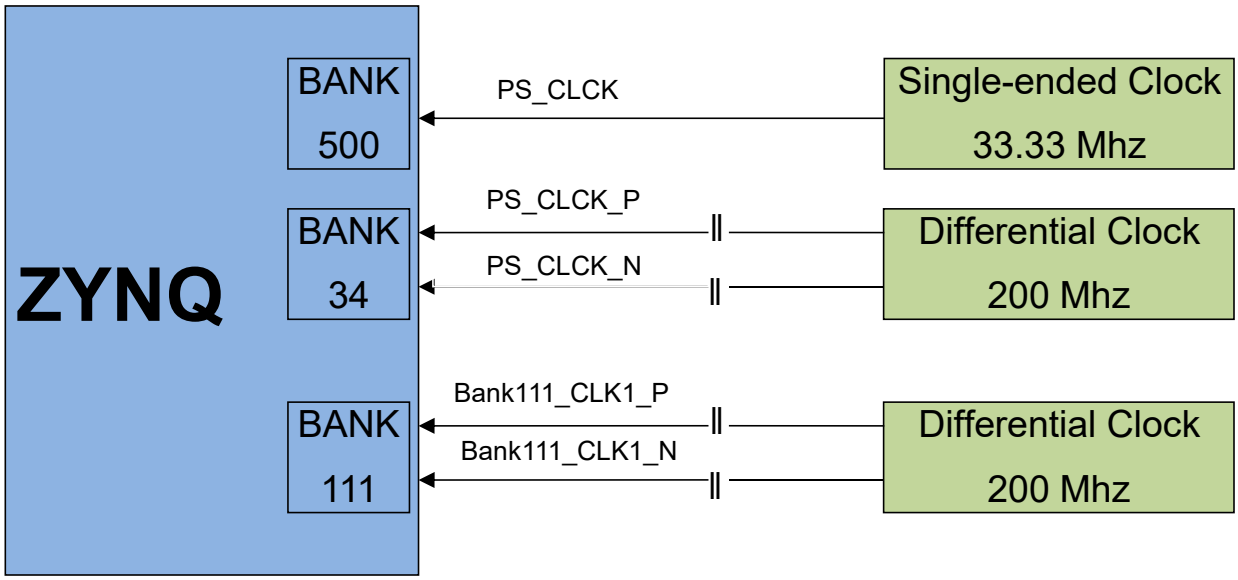

Figure 2-6-1: Clock source in the Core Board

PS system clock source

The ZYNQ chip provides a 33.333MHz clock input to the PS section via the X4 crystal on the FPGA core board AC7Z035. The input of the clock is connected to the pin of the PS_CLK_500 of the BANK500 of the ZYNQ chip. The schematic diagram is shown in Figure 2-6-2:

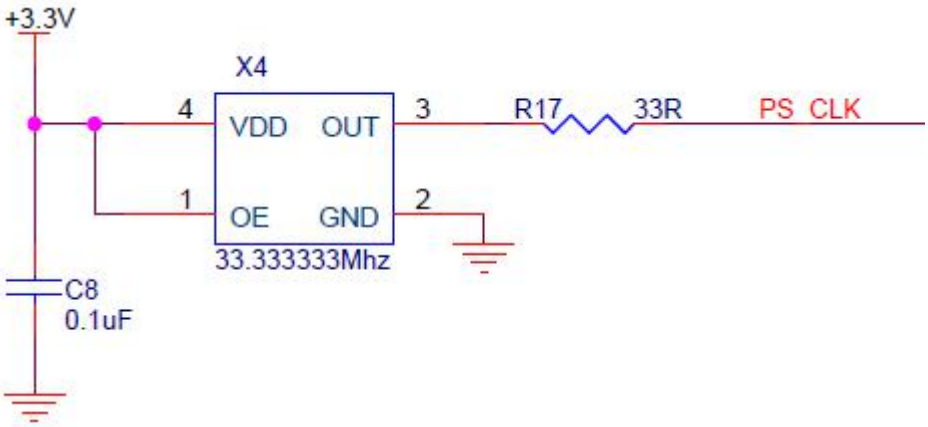

Figure 2-6-2: Active crystal oscillator to the PS section

PS Clock Pin Assignment

Signal Name	ZYNQ Pin
PS_CLK	B24

PL system clock source

The differential 200MHz PL system clock source is provided on the FPGA core board AC7Z035 for the reference clock of the DDR3 controller. The crystal output is connected to the global clock (MRCC) of the FPGA BANK34, which can be used to drive the DDR3 controller and user logic in the FPGA. The schematic diagram of the clock source is shown in Figure 2-6-3

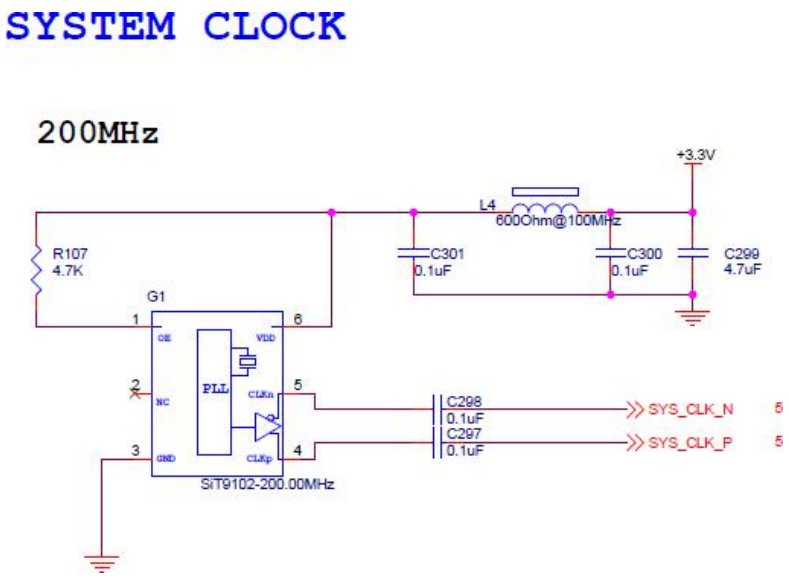

Figure 2-6-3: PL system clock source

PL Clock pin assignment:

Signal Name	ZYNQ Pin
SYS_CLK_P	C8
SYS_CLK_N	C7

GTX reference clock

The FPGA core board AC7Z035 provides a 125Mhz reference clock for the GTX transceiver. The reference clock is connected to the reference clock input of the BANK111, REFCLK1P/REFCLK1N. The schematic diagram of the clock source is shown in Figure 2-6-4.

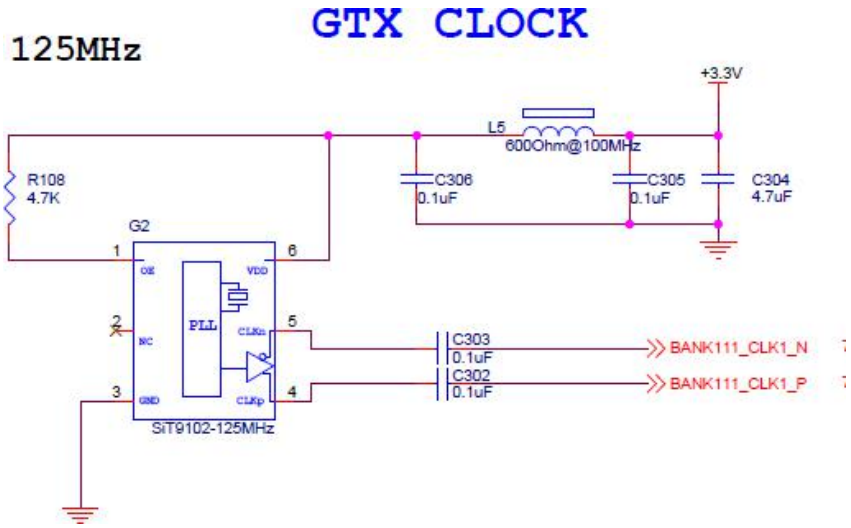

Figure 2-6-4: GTX Clock Source

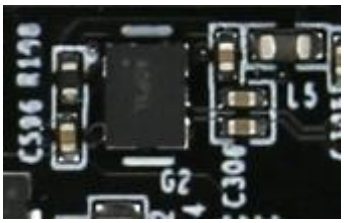

Figure 2-6-5: Programmable Clock Source on the AX7Z035 FPGA Core Board

GTX clock source ZYNQ pin assignment:：

Signal Name	ZYNQ Pin
BANK111_CLK1_P	AA6
BANK111_CLK1_N	AA5

Part 1.7: LED Light

There are 3 red LED lights on the AC7Z035 FPGA core board, one of which is the power indicator light (PWR), one is the configuration LED light (DONE), and one is the user LED light. When the core board is powered, the power indicator will illuminate; when the FPGA is configured, the configuration LED will illuminate. The user LED light is connected to the IO of the PL. The user can control the light on and off by the program. When the IO voltage connected to the user LED is high, the user LED is off. When the connection IO voltage is low, the user LED will be lit. The schematic diagram of the LED light

hardware connection is shown in Figure 2-7-1:

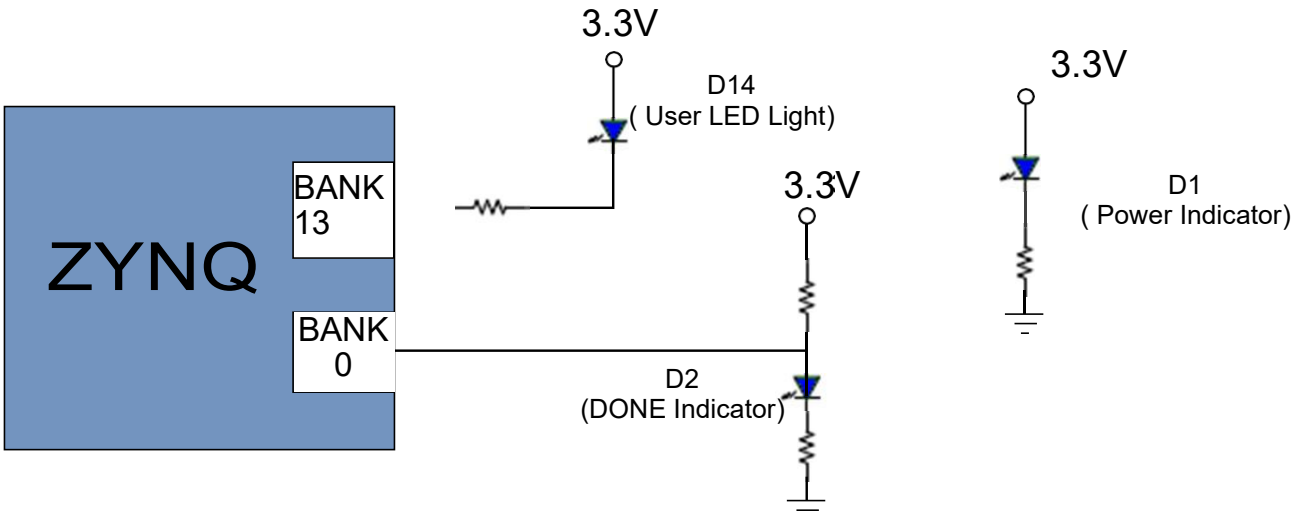

Figure 2-7-1: AC7Z035 FPGA Core board LED light Hardware Connection

Pin assignment of user LEDs

LED Light	ZYNQ Pin Name	ZYNQ Pin Number	Description
D14	B13_IO25	V19	User LED Light

Part 1.8: Reset circuit

There is a reset circuit on the AC7Z035 core board. The reset input signal is connected to the reset button on the carrier board. The reset output is connected to the PS reset pin of the ZYNQ chip. The user can use the buttons on the carrier board to reset the ZYNQ system. The schematic diagram of the reset connection is shown in Figure 2-8-1:

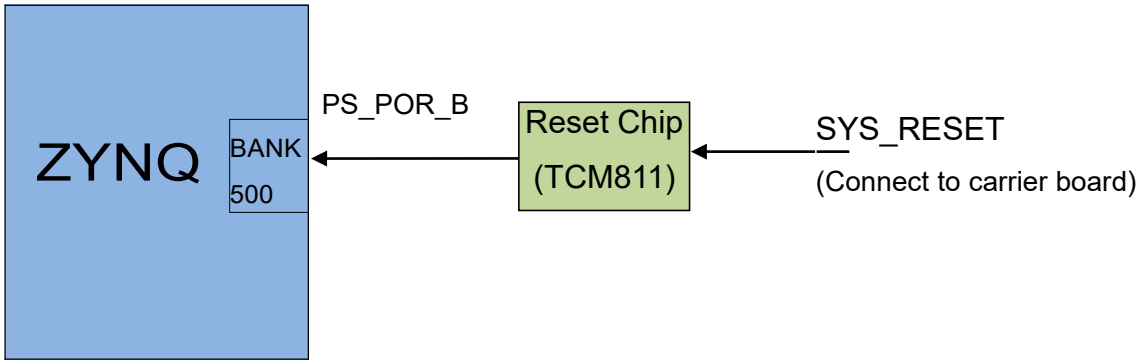

Figure 2-8-1: Reset circuit connection diagram

Reset button ZYNQ pin assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_POR_B	PS_POR_B_500	A22	ZYNQ System Reset Signal

Part 1.9: Power Supply

The AC7Z035 FPGA core board is powered by DC5V and is powered by a connection carrier board. The power supply design diagram on the FPGA board is shown in Figure 2-9-1

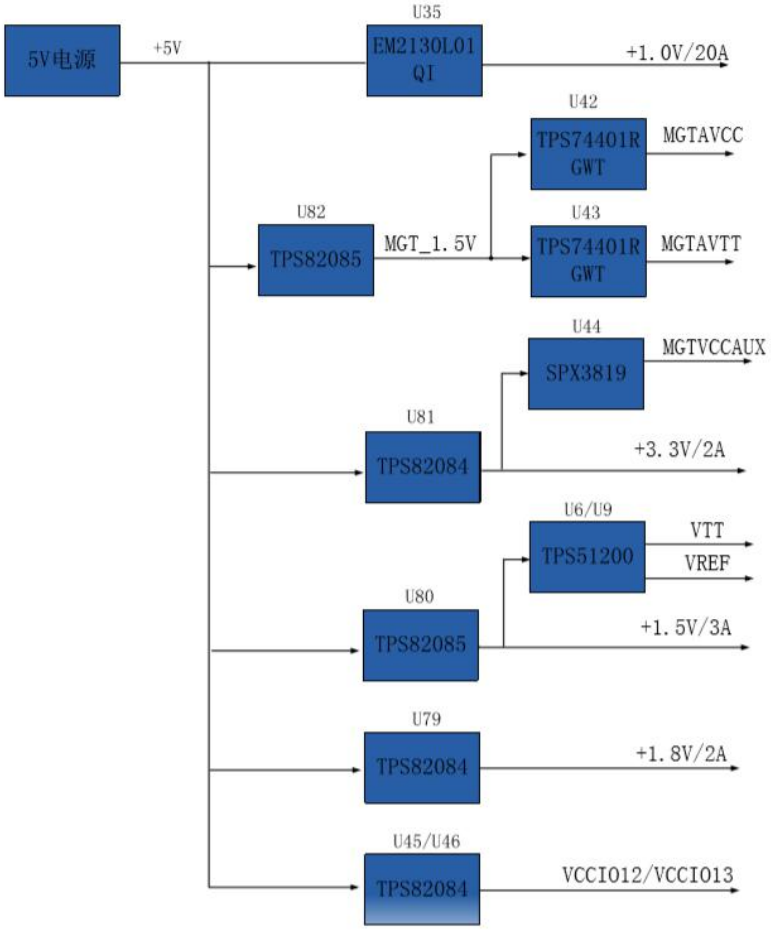

Figure 2-9-1：Power interface section in the schematic

+5V generates +1.0V ZYNQ core power through DCDC power chip EM2130L01QI. EM2130 output current is up to 20A, which is enough to meet the current demand of ZYNQ core voltage. The +5V power supply then uses the DCDC chip TPS82084 and TPS82085 to generate four power supplies:

+1.5V, +3.3V, MGT_1.5V and +1.5V. The MGT_1.5V power supply generates +1.0V and +1.2V power supplies for GTX through two LDO chips TPS74401, and +3.3V generates GTX auxiliary power +1.8V through an LDO chip SPX3819-1-8. The VTT and VREF voltages of the DDR3 of the PS section and the PL section are generated by U6, U9. In addition, the IO power supply of BANK12 and BANK13 is generated by two SPX3819M5-3-3. Users can change the IO input and output of these two BANKs to other voltage standards by replacing the LDO chip.

The functions of each power distribution are shown in the following table:：

Power Supply	Function
+1.0V	ZYNQ PS and PL section Core Voltage
+1.8V	ZYNQ PS and PL partial auxiliary voltage,BANK501, BANK35, eMMC
+3.3V	ZYNQ Bank0,Bank500，QSIP FLASH, Clock Crystal
+1.5V	DDR3, ZYNQ Bank501, Bank33,Bank34,
VCCIO12	ZYNQ Bank12
VCCIO13	ZYNQ Bank13
VREF,VTT(+0.75V)	PS DDR3，PL DDR3
MGTAVCC(+1.0V)	ZYNQ Bank111, Bank112
MGTAVTT(+1.2V)	ZYNQ Bank111, Bank112
MGTVCCAUX(+1.8V)	ZYNQ Bank111, Bank112

Because the power supply of the ZYNQ FPGA has the power-on sequence requirements, in the circuit design, we have designed according to the power requirements of the chip. The power-on sequence is +1.0V->+1.8V->(+1.5 V, +3.3V, VCCIO12,VCCIO13) circuit design to ensure the normal operation of the chip.

The physical diagram of the power circuit on the AX7Z035 core board is shown in Figure 2-9-2:

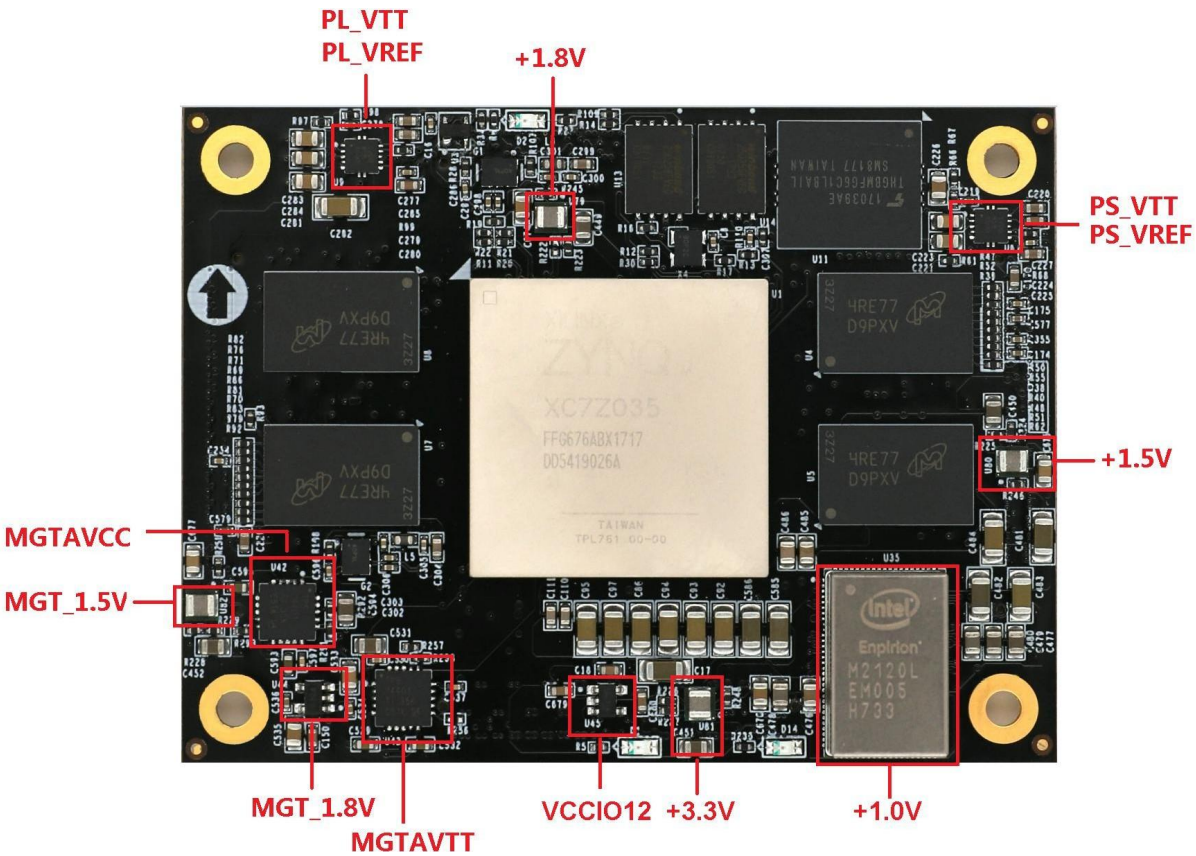

Figure 2-9-2: Power Supply on the AX7Z035 Core Board

Part 1.10: AC7Z035 Core Board Size Dimension

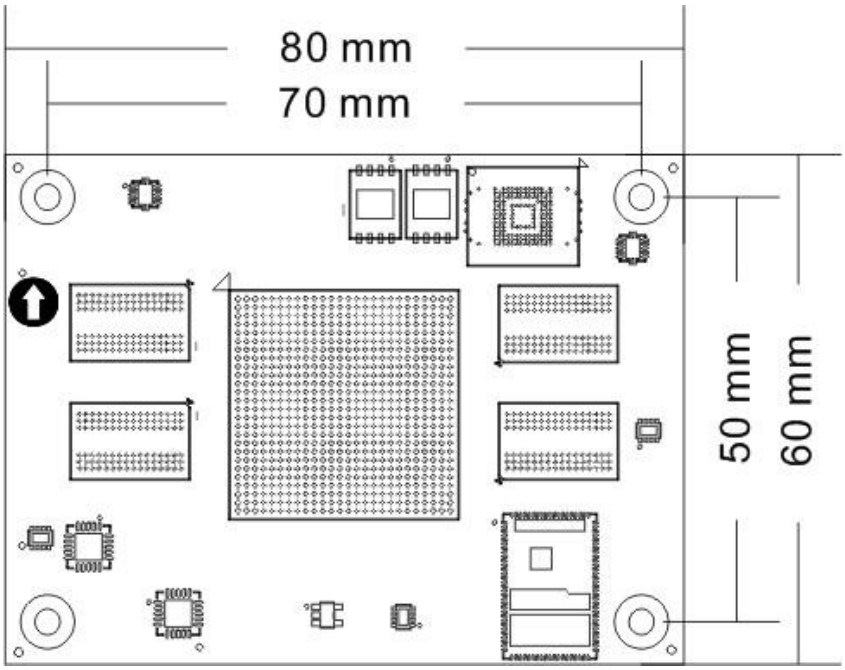

Figure 2-10-1: AC7Z035 Core Board Size Dimension

Part 1.11: Board to Board Connectors pin assignment

The core board has a total of four high-speed expansion ports. It uses four 120-pin inter-board connectors (J29~J32) to connect to the carrier board. The connector uses the Panasonic AXK5A2147YG, and the connector type corresponding to the carrier board is AXK6A2337YG. J29 connects BANK12 IO and BANK13 IO, J30 connects GTX transceiver signal, J31 connects JTAG and BANK35 IO (1.8V level standard), J32 connects PS MIO, BANK13 IO and +5V power supply

Pin assignment of J29 connector

J29 Pin	Signal Name	ZYNQ Pin Number	J29 Pin	Signal Name	ZYNQ Pin Number
1	B13_L8_P	AE23	2	B13_L9_N	AB22
3	B13_L8_N	AF23	4	B13_L9_P	AB21
5	GND	-	6	GND	-
7	B13_L10_N	AA23	8	B13_L13_N	AD21
9	B13_L10_P	AA22	10	B13_L13_P	AD20
11	GND	-	12	GND	-
13	B13_L15_N	AF20	14	B13_L14_N	AC22
15	B13_L15_P	AF19	16	B13_L14_P	AC21
17	GND	-	18	GND	-
19	B13_L23_N	W19	20	B13_L7_P	AE22
21	B13_L23_P	W18	22	B13_L7_N	AF22
23	GND	-	24	GND	-
25	B13_L22_P	AA19	26	B13_L20_P	AA20
27	B13_L22_N	AB19	28	B13_L20_N	AB20
29	GND	-	30	GND	-
31	B13_L17_N	AD19	32	B13_L18_N	AF18
33	B13_L17_P	AD18	34	B13_L18_P	AE18
35	GND	-	36	GND	-
37	B13_L19_N	Y20	38	B13_L16_N	AE21

39	B13_L19_P	W20	40	B13_L16_P	AE20
41	GND	-	42	GND	-
43	B13_L24_N	AA18	44	B13_L21_N	AC19
45	B13_L24_P	Y18	46	B13_L21_P	AC18
47	GND	-	48	GND	-
49	B12_L23_P	Y16	50	B12_L18_N	AF17
51	B12_L23_N	Y15	52	B12_L18_P	AE17
53	GND	-	54	GND	-
55	B12_L15_P	AD16	56	B12_L16_P	AF15
57	B12_L15_N	AD15	58	B12_L16_N	AF14
59	GND	-	60	GND	-
61	B12_L14_P	AB15	62	B12_L13_N	AD14
63	B12_L14_N	AB14	64	B12_L13_P	AC14
65	GND	-	66	GND	-
67	B12_L10_N	AF13	68	B12_L19_P	Y17
69	B12_L10_P	AE13	70	B12_L19_N	AA17
71	GND	-	72	GND	-
73	B12_L4_P	AB11	74	B12_L20_P	AB17
75	B12_L4_N	AB10	76	B12_L20_N	AB16
77	GND	-	78	GND	-
79	B12_L7_P	AE10	80	B12_L8_N	AF12
81	B12_L7_N	AD10	82	B12_L8_P	AE12
83	GND	-	84	GND	-
85	B12_L24_P	W16	86	B12_L21_P	AC17
87	B12_L24_N	W15	88	B12_L21_N	AC16
89	GND	-	90	GND	-
91	B12_L3_N	AA10	92	B12_L17_P	AE16
93	B12_L3_P	Y10	94	B12_L17_N	AE15
95	GND	-	96	GND	-
97	B12_L11_P	AC12	98	B12_L22_P	AA15
99	B12_L11_N	AD11	100	B12_L22_N	AA14
101	GND	-	102	GND	-

103	B12_L12_N	AD13	104	B12_L5_P	W13
105	B12_L12_P	AC13	106	B12_L5_N	Y13
107	GND	-	108	GND	-
109	B12_L6_P	AA13	110	B12_L9_P	AE11
111	B12_L6_N	AA12	112	B12_L9_N	AF10
113	GND	-	114	GND	-
115	B12_L1_P	Y12	116	B12_L2_P	AB12
117	B12_L1_N	Y11	118	B12_L2_N	AC11
119	GND	-	120	GND	-

Pin assignment of J30 connector

J30 Pin	Signal Name	ZYNQ Pin Number	J30 Pin	Signal Name	ZYNQ Pin Number
1			2		
3			4		
5	GND	-	6	GND	-
7			8		
9			10		
11	GND	-	12	GND	-
13			14		
15			16		
17	GND	-	18	GND	-
19			20		
21			22		
23	GND	-	24	GND	-
25			26		
27			28		
29	GND	-	30	GND	-
31	BANK112_TX0_N	AA1	32	BANK112_RX0_N	AB3
33	BANK112_TX0_P	AA2	34	BANK112_RX0_P	AB4
35	GND	R13	36	GND	R13

37	BANK112_TX1_N	W1	38	BANK112_RX1_N	Y3
39	BANK112_TX1_P	W2	40	BANK112_RX1_P	Y4
41	GND	R13	42	GND	R13
43	BANK112_TX2_N	U1	44	BANK112_RX2_N	V3
45	BANK112_TX2_P	U2	46	BANK112_RX2_P	V4
47	GND	R13	48	GND	R13
49	BANK112_TX3_N	R1	50	BANK112_RX3_N	T3
51	BANK112_TX3_P	R2	52	BANK112_RX3_P	T4
53	GND	R13	54	GND	R13
55	BANK112_CLK0_N	R5	56	BANK112_CLK1_N	U5
57	BANK112_CLK0_P	R6	58	BANK112_CLK1_P	U6
59	GND	-	60	GND	R13
61			62	BANK111_RX3_N	AD3
63			64	BANK111_RX3_P	AD4
65	GND	-	66	GND	R13
67			68	BANK111_TX3_N	AC1
69			70	BANK111_TX3_P	AC2
71	GND	-	72	GND	R13
73			74	BANK111_RX2_N	AC5
75			76	BANK111_RX2_P	AC6
77	GND	-	78	GND	R13
79			80	BANK111_TX2_N	AE1
81			82	BANK111_TX2_P	AE2
83	GND	-	84	GND	R13
85			86	BANK111_RX1_N	AE5
87			88	BANK111_RX1_P	AE6
89	GND	-	90	GND	R13
91			92	BANK111_TX1_N	AF3
93			94	BANK111_TX1_P	AF4
95	GND	-	96	GND	R13
97			98	BANK111_RX0_N	AD7
99			100	BANK111_RX0_P	AD8

101	GND	-	102	GND	R13
103			104	BANK111_TX0_N	AF7
105			106	BANK111_TX0_P	AF8
107	GND	-	108	GND	R13
109			110	BANK111_CLK0_N	W5
111			112	BANK111_CLK0_P	W6
113	GND	-	114	GND	-
115			116		
117			118		
119	GND	-	120	GND	-

Pin assignment of J31 connector

J31 Pin	Signal Name	ZYNQ Pin Number	J31 Pin	Signal Name	ZYNQ Pin Number
1	FPGA_TCK	W12	2	FPGA_TDI	V11
3	FPGA_TMS	W11	4	FPGA_TDO	W10
5	GND	-	6	GND	-
7	B35_L3_P	G10	8	B35_L2_P	E10
9	B35_L3_N	F10	10	B35_L2_N	D10
11	GND	-	12	GND	-
13	B35_L7_N	H12	14	B35_L6_P	F13
15	B35_L7_P	H13	16	B35_L6_N	E13
17	GND	-	18	GND	-
19	B35_L4_P	E11	20	B35_L23_P	C11
21	B35_L4_N	D11	22	B35_L23_N	B11
23	GND	-	24	GND	-
25	B35_L5_N	G11	26	B35_L22_P	C12
27	B35_L5_P	G12	28	B35_L22_N	B12
29	GND	-	30	GND	-
31	B35_L8_P	K13	32	B35_L24_N	A12
33	B35_L8_N	J13	34	B35_L24_P	A13

35	GND	-	36	GND	-
37	B35_L12_P	J14	38	B35_L11_N	F14
39	B35_L12_N	H14	40	B35_L11_P	G14
41	GND	-	42	GND	-
43	B35_L9_P	K15	44	B35_L19_N	C13
45	B35_L9_N	J15	46	B35_L19_P	D13
47	GND	-	48	GND	-
49	B35_L1_N	E12	50	B35_L21_N	A14
51	B35_L1_P	F12	52	B35_L21_P	A15
53	GND	-	54	GND	-
55	B35_L17_N	B15	56	B35_L14_P	F15
57	B35_L17_P	B16	58	B35_L14_N	E15
59	GND	-	60	GND	-
61	B35_L20_N	B14	62	B35_L18_P	B17
63	B35_L20_P	C14	64	B35_L18_N	A17
65	GND	-	66	GND	-
67	B35_L10_N	G15	68	B35_L15_N	C16
69	B35_L10_P	G16	70	B35_L15_P	C17
71	GND	-	72	GND	-
73	B35_L13_N	D14	74		
75	B35_L13_P	D15	76		
77	GND	-	78	GND	-
79	B35_L16_N	D16	80		
81	B35_L16_P	E16	82		
83	GND	-	84	GND	-
85			86		
87			88		
89	GND	-	90	GND	-
91			92		
93			94		
95	GND	-	96	GND	-
97			98		

99			100		
101	GND	-	102	GND	-
103			104		
105			106		
107	GND	-	108	GND	-
109			110		
111			112		
113	GND	-	114	GND	-
115			116		
117	SYS_RESET	-	118		
119	GND	-	120	GND	-

Pin assignment of J32 connector

J32 Pin	Signal Name	ZYNQ Pin Number	J32 Pin	Signal Name	ZYNQ Pin Number
1	PS_MIO5	C26	2	PS_MIO17	G17
3	PS_MIO4	F24	4	PS_MIO18	G20
5	GND	-	6	GND	-
7	PS_MIO14	D23	8	PS_MIO19	G19
9	PS_MIO15	C24	10	PS_MIO20	H19
11	GND	-	12	GND	-
13	PS_MIO52	A20	14	PS_MIO16	G21
15	PS_MIO53	A19	16	PS_MIO21	F22
17	GND	-	18	GND	-
19	PS_MIO7	E23	20	PS_MIO26	H17
21			22	PS_MIO25	F19
23	GND	-	24	GND	-
25	PS_MIO40	C22	26	PS_MIO24	J19
27	PS_MIO41	C19	28	PS_MIO23	F20
29	GND	-	30	GND	-

31	PS_MIO42	F17	32	PS_MIO27	F18
33	PS_MIO43	D18	34	PS_MIO22	G22
35	GND	-	36	GND	-
37	PS_MIO44	E18	38	PS_MIO30	K19
39	PS_MIO45	C18	40	PS_MIO29	E20
41	GND	-	42	GND	-
43			44	PS_MIO36	K16
45			46	PS_MIO31	E21
47	GND	-	48	GND	-
49			50	PS_MIO32	K17
51			52	PS_MIO33	E22
53	GND	-	54	GND	-
55			56	PS_MIO34	J16
57			58	PS_MIO35	D19
59	GND	-	60	GND	-
61			62	PS_MIO28	J18
63			64	PS_MIO37	D20
65	GND	-	66	GND	-
67			68	PS_MIO38	D21
69			70	PS_MIO39	C21
71	GND	-	72	GND	-
73			74		
75			76		
77	GND	-	78	GND	-
79			80		
81			82		
83	GND	-	84	GND	-
85	B13_L1_P	AA25	86	B13_L11_P	AD23
87	B13_L1_N	AB25	88	B13_L11_N	AD24
89	GND	-	90	GND	-
91	B13_L6_P	AA24	92	B13_L4_P	AD25
93	B13_L6_N	AB24	94	B13_L4_N	AD26

95	GND	-	96	GND	-
97	B13_L2_N	AC26	98	B13_L5_P	AF24
99	B13_L2_P	AB26	100	B13_L5_N	AF25
101	GND	-	102	GND	-
103	B13_L12_P	AC23	104	B13_L3_P	AE25
105	B13_L12_N	AC24	106	B13_L3_N	AE26
107	+5V	-	108	+5V	-
109	+5V	-	110	+5V	-
111	+5V	-	112	+5V	-
113	+5V	-	114	+5V	-
115	+5V	-	116	+5V	-
117	+5V	-	118	+5V	-
119	+5V	-	120	+5V	-