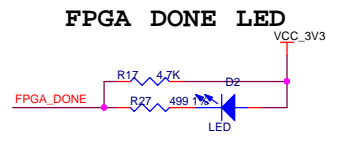
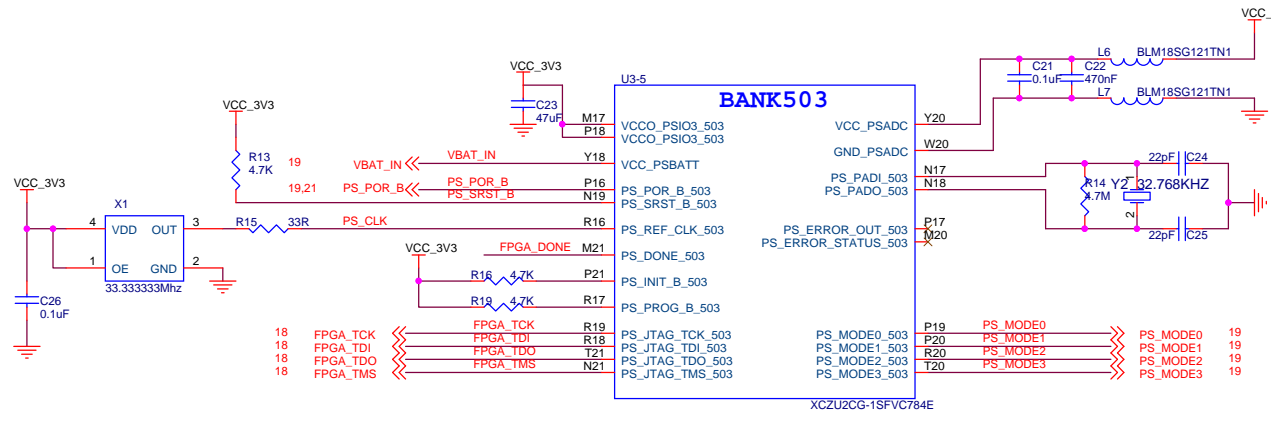
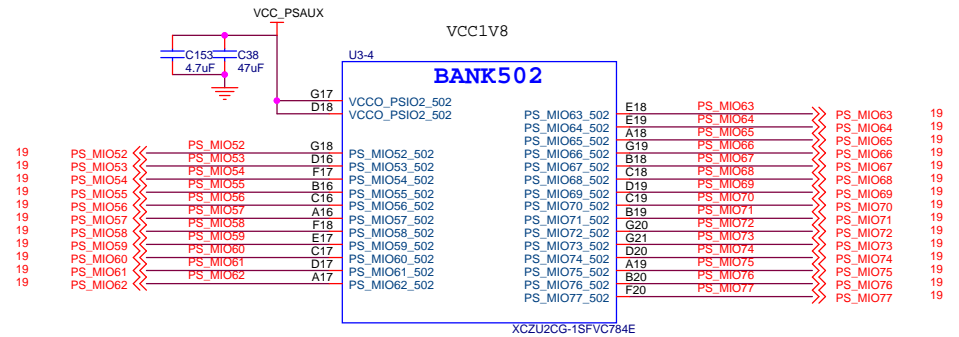
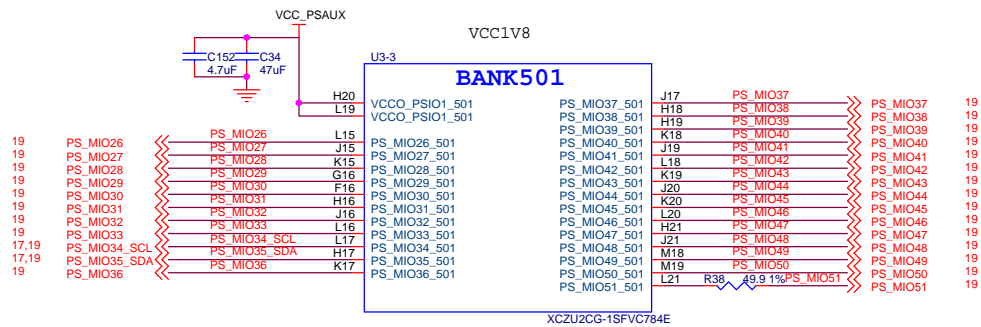
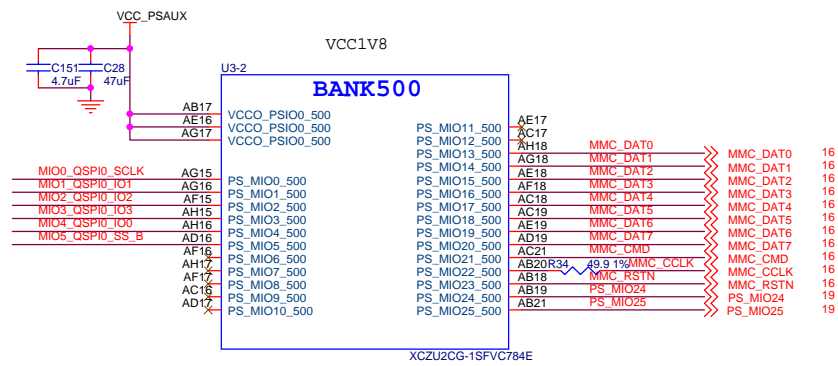
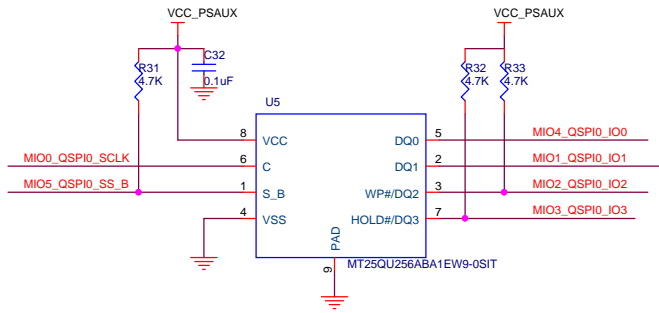
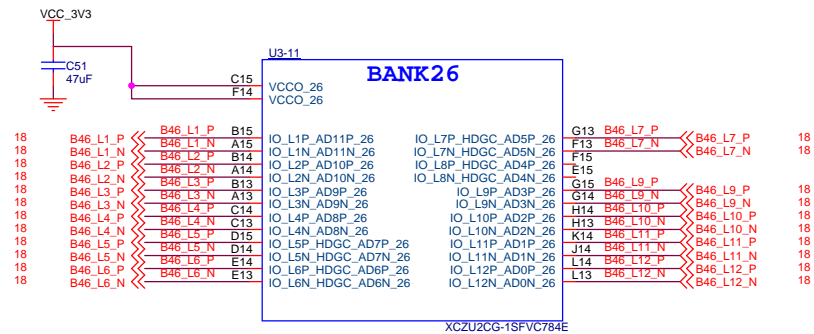
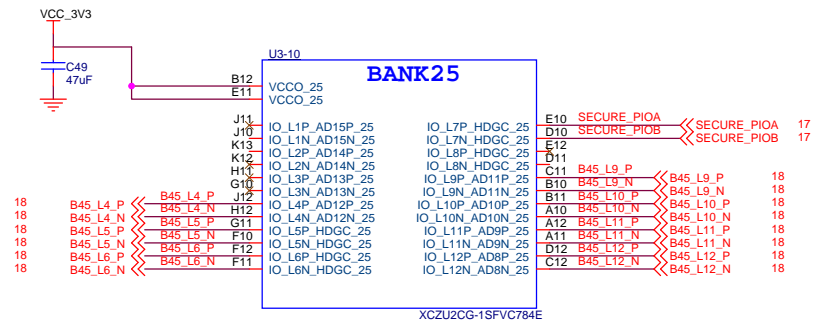
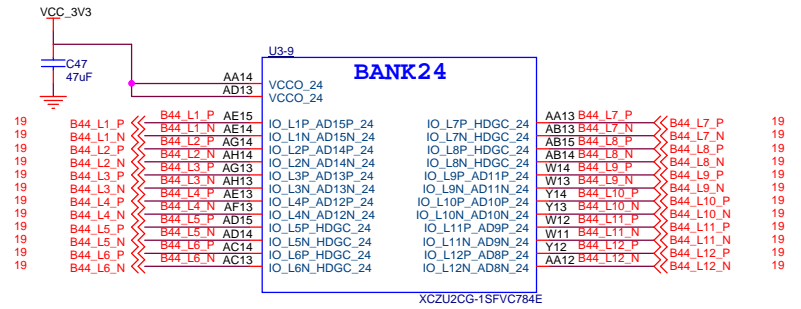
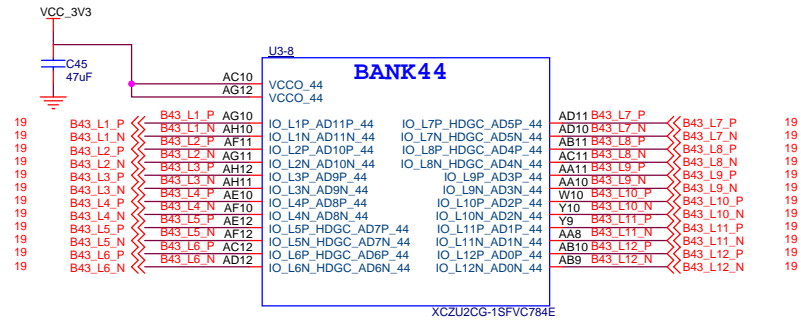
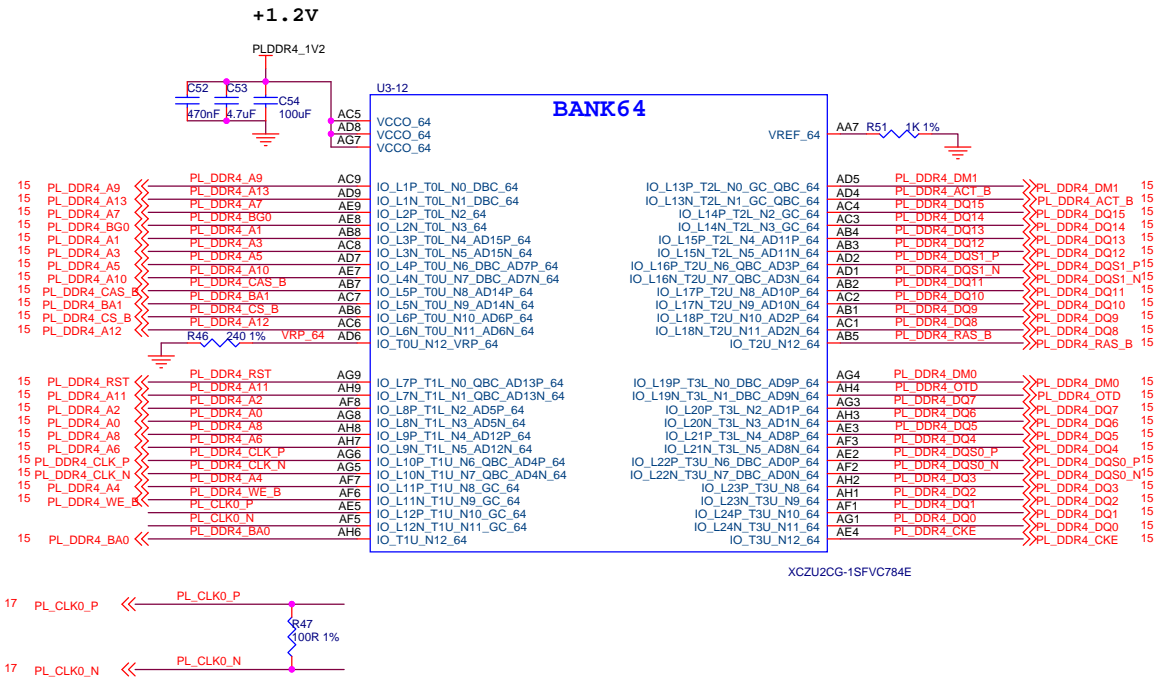


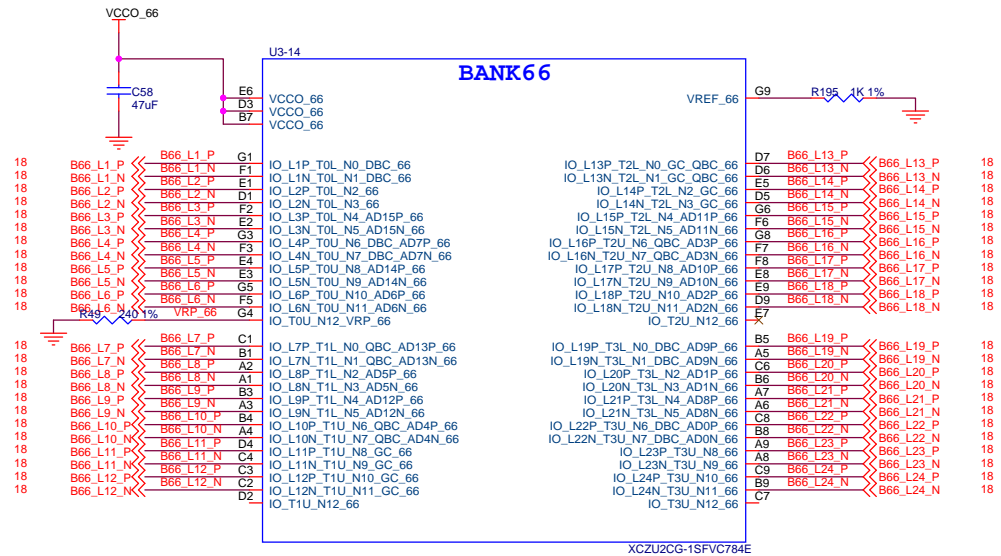
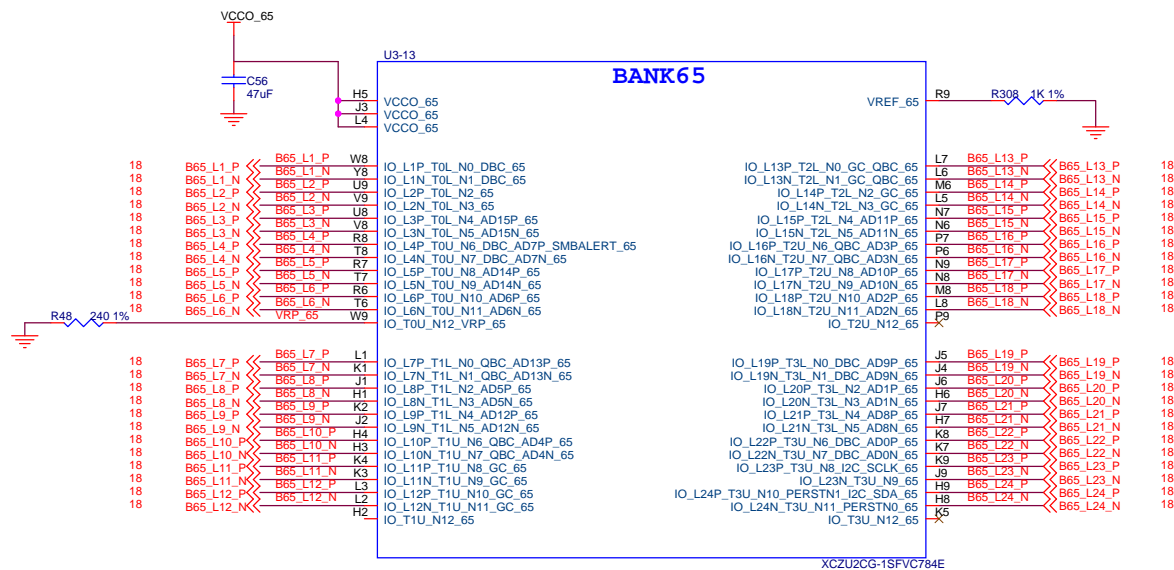
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0000	PS JTAG	PS JTAG Interface
0001	Quad SPI(24b)	24-Bit addresssing(QSPI24)
0010	Quad SPI(32b)	32-Bit addresssing(QSPI32)
0011	SD0(2.0)	SD2.0
0100	NAND	Requires 8-bit data bus width
0101	SD1(2.0)	SD2.0
0110	eMMC(1.8V)	eMMC version 4.5 at 1.8V
0111	USB0(2.0)	USB 2.0 only
1000	PJTAG(MIO #0)	PJTAG connection 0 option
1001	PJTAG(MIO #1)	PJTAG connection 1 option
1110	SD1 LS(3.0)	SD 3.0

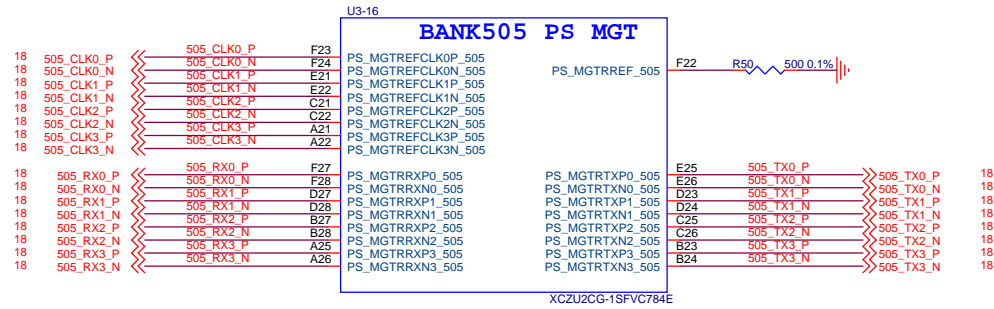


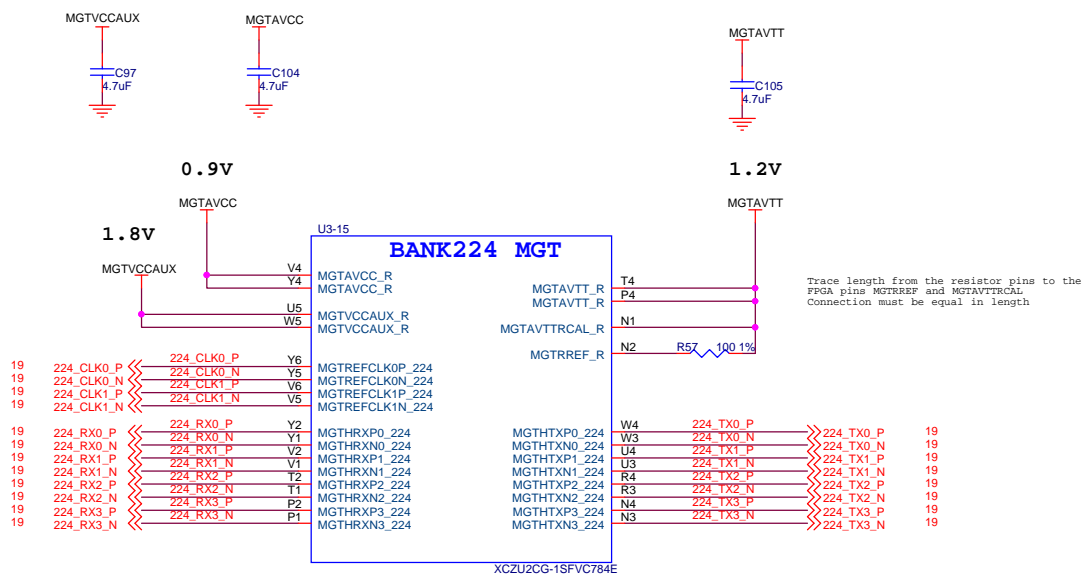


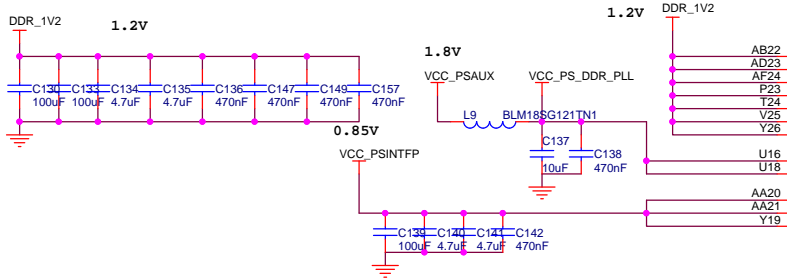












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VCCO_PSSDDR_504	PS_DDR_CK0_504	W25 PS_DDR4_CLK0_P	>> PS_DDR4_CLK0_P	11,12,13,14
PS_PSSDDR_504	PS_DDR_CK_NO_504	W26 PS_DDR4_CLK0_N	>> PS_DDR4_CLK0_N	11,12,13,14
VCCO_PSSDDR_504	PS_PSSDDR_504	W28 PS_DDR4_CKE0	>> PS_DDR4_CKE0	11,12,13,14
VCCO_PSSDDR_504	PS_PSSDDR_504			
VCCO_PSSDDR_504	PS_PSSDDR_504			
VCCO_PSSDDR_504	PS_PSSDDR_504			
VCCO_PSSDDR_504	PS_PSSDDR_504			
VCCO_PSSDDR_504	PS_PSSDDR_504			
VCCO_PSSDDR_504	PS_PSSDDR_504			
VCCO_PSSDDR_504	PS_PSSDDR_504			
VCC_PSSDDR_PLL	PS_DDR_A0_504	W28 PS_DDR4_A0	>> PS_DDR4_A0	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A1_504	Y28 PS_DDR4_A1	>> PS_DDR4_A1	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A2_504	AB28 PS_DDR4_A2	>> PS_DDR4_A2	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A3_504	AA28 PS_DDR4_A3	>> PS_DDR4_A3	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A4_504	Y27 PS_DDR4_A4	>> PS_DDR4_A4	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A5_504	AA27 PS_DDR4_A5	>> PS_DDR4_A5	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A6_504	Y27 PS_DDR4_A6	>> PS_DDR4_A6	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A7_504	Y27 PS_DDR4_A7	>> PS_DDR4_A7	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A8_504	AA27 PS_DDR4_A8	>> PS_DDR4_A8	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A9_504	AA23 PS_DDR4_A9	>> PS_DDR4_A9	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A10_504	AA25 PS_DDR4_A10	>> PS_DDR4_A10	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A11_504	AA26 PS_DDR4_A11	>> PS_DDR4_A11	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A12_504	AA25 PS_DDR4_A12	>> PS_DDR4_A12	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A13_504	AA23 PS_DDR4_A13	>> PS_DDR4_A13	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A14_504	AA22 PS_DDR4_A14	>> PS_DDR4_A14	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A15_504	AB23 PS_DDR4_A15	>> PS_DDR4_A15	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A16_504	AA26 PS_DDR4_A16	>> PS_DDR4_A16	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A17_504	AA25 PS_DDR4_A17	>> PS_DDR4_A17	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_A17_504	AC22		
VCC_PSSDDR_PLL	PS_DDR_CS_NO_504	W27 PS_DDR4_CS0_B	>> PS_DDR4_CS0_B	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_CS_N1_504	W26		
VCC_PSSDDR_PLL	PS_DDR_BA0_504	V23 PS_DDR4_BA0	>> PS_DDR4_BA0	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_BA1_504	W22 PS_DDR4_BA1	>> PS_DDR4_BA1	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_BG0_504	W24 PS_DDR4_BG0	>> PS_DDR4_BG0	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_BG1_504	W22		
VCC_PSSDDR_PLL	PS_DDR_PARITY_504	V24 PS_DDR4_PARITY	>> PS_DDR4_PARITY	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_RAM_RST_N_504	U23 PS_DDR4_RESET_B	>> PS_DDR4_RESET_B	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_ACT_N_504	Y23 PS_DDR4_ACT_B	>> PS_DDR4_ACT_B	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_ALERT_N_504	U25 PS_DDR4_ALERT_B	>> PS_DDR4_ALERT_B	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_ZQ_504	U24 PS_DDR4_ZQ	R58 240 1%	
VCC_PSSDDR_PLL	PS_DDR_ODT0_504	U28 PS_DDR4_ODT0	>> PS_DDR4_ODT0	11,12,13,14
VCC_PSSDDR_PLL	PS_DDR_ODT1_504	U26		

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11 PS_DDR4_DQ0	PS_DDR4_DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504	T22 PS_DDR4_DQ32	>> PS_DDR4_DQ32	13
11 PS_DDR4_DQ1	PS_DDR4_DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504	R22 PS_DDR4_DQ33	>> PS_DDR4_DQ33	13
11 PS_DDR4_DQ2	PS_DDR4_DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504	P22 PS_DDR4_DQ34	>> PS_DDR4_DQ34	13
11 PS_DDR4_DQ3	PS_DDR4_DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504	N22 PS_DDR4_DQ35	>> PS_DDR4_DQ35	13
11 PS_DDR4_DQ4	PS_DDR4_DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504	T23 PS_DDR4_DQ36	>> PS_DDR4_DQ36	13
11 PS_DDR4_DQ5	PS_DDR4_DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504	M23 PS_DDR4_DQ37	>> PS_DDR4_DQ37	13
11 PS_DDR4_DQ6	PS_DDR4_DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504	R24 PS_DDR4_DQ38	>> PS_DDR4_DQ38	13
11 PS_DDR4_DQ7	PS_DDR4_DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504	N24 PS_DDR4_DQ39	>> PS_DDR4_DQ39	13
11 PS_DDR4_DQ8	PS_DDR4_DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504	H24 PS_DDR4_DQ40	>> PS_DDR4_DQ40	14
11 PS_DDR4_DQ9	PS_DDR4_DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504	J24 PS_DDR4_DQ41	>> PS_DDR4_DQ41	14
11 PS_DDR4_DQ10	PS_DDR4_DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504	M24 PS_DDR4_DQ42	>> PS_DDR4_DQ42	14
11 PS_DDR4_DQ11	PS_DDR4_DQ11	AD22	PS_DDR_DQ11_504	PS_DDR_DQ43_504	K24 PS_DDR4_DQ43	>> PS_DDR4_DQ43	14
11 PS_DDR4_DQ12	PS_DDR4_DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504	J22 PS_DDR4_DQ44	>> PS_DDR4_DQ44	14
11 PS_DDR4_DQ13	PS_DDR4_DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504	H22 PS_DDR4_DQ45	>> PS_DDR4_DQ45	14
11 PS_DDR4_DQ14	PS_DDR4_DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504	K22 PS_DDR4_DQ46	>> PS_DDR4_DQ46	14
11 PS_DDR4_DQ15	PS_DDR4_DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504	L22 PS_DDR4_DQ47	>> PS_DDR4_DQ47	14
11 PS_DDR4_DQ16	PS_DDR4_DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504	M25 PS_DDR4_DQ48	>> PS_DDR4_DQ48	13
12 PS_DDR4_DQ17	PS_DDR4_DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504	M26 PS_DDR4_DQ49	>> PS_DDR4_DQ49	13
12 PS_DDR4_DQ18	PS_DDR4_DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504	L25 PS_DDR4_DQ50	>> PS_DDR4_DQ50	13
12 PS_DDR4_DQ19	PS_DDR4_DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504	L26 PS_DDR4_DQ51	>> PS_DDR4_DQ51	13
12 PS_DDR4_DQ20	PS_DDR4_DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504	K28 PS_DDR4_DQ52	>> PS_DDR4_DQ52	13
12 PS_DDR4_DQ21	PS_DDR4_DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504	L28 PS_DDR4_DQ53	>> PS_DDR4_DQ53	13
12 PS_DDR4_DQ22	PS_DDR4_DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504	M28 PS_DDR4_DQ54	>> PS_DDR4_DQ54	13
12 PS_DDR4_DQ23	PS_DDR4_DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504	N28 PS_DDR4_DQ55	>> PS_DDR4_DQ55	13
12 PS_DDR4_DQ24	PS_DDR4_DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504	J28 PS_DDR4_DQ56	>> PS_DDR4_DQ56	13
12 PS_DDR4_DQ25	PS_DDR4_DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504	K27 PS_DDR4_DQ57	>> PS_DDR4_DQ57	14
12 PS_DDR4_DQ26	PS_DDR4_DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504	H28 PS_DDR4_DQ58	>> PS_DDR4_DQ58	14
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12 PS_DDR4_DQ31	PS_DDR4_DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504	J25 PS_DDR4_DQ63	>> PS_DDR4_DQ63	14
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11 PS_DDR4_QS0_N	PS_DDR4_QS0_N	AG21	PS_DDR_QS_N0_504	PS_DDR_DQ65_504	P28		
11 PS_DDR4_QS1_P	PS_DDR4_QS1_P	AF23	PS_DDR_QS_P1_504	PS_DDR_DQ66_504	P27		
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12 PS_DDR4_QS3_N	PS_DDR4_QS3_N	AF27	PS_DDR_QS_N3_504	PS_DDR_DQ71_504	P25		
13 PS_DDR4_QS4_P	PS_DDR4_QS4_P	N23	PS_DDR_QS_P4_504	PS_DDR_DM0_504	AG20 PS_DDR4_DM0	>> PS_DDR4_DM0	11
13 PS_DDR4_QS4_N	PS_DDR4_QS4_N	M23	PS_DDR_QS_N4_504	PS_DDR_DM1_504	AE23 PS_DDR4_DM1	>> PS_DDR4_DM1	11
14 PS_DDR4_QS5_P	PS_DDR4_QS5_P	L23	PS_DDR_QS_P5_504	PS_DDR_DM2_504	AE25 PS_DDR4_DM2	>> PS_DDR4_DM2	12
14 PS_DDR4_QS5_N	PS_DDR4_QS5_N	K23	PS_DDR_QS_N5_504	PS_DDR_DM3_504	AE28 PS_DDR4_DM3	>> PS_DDR4_DM3	12
13 PS_DDR4_QS6_P	PS_DDR4_QS6_P	N26	PS_DDR_QS_P6_504	PS_DDR_DM4_504	R23 PS_DDR4_DM4	>> PS_DDR4_DM3	12
13 PS_DDR4_QS6_N	PS_DDR4_QS6_N	N27	PS_DDR_QS_N6_504	PS_DDR_DM5_504	H23 PS_DDR4_DM5	>> PS_DDR4_DM4	14
13 PS_DDR4_QS7_P	PS_DDR4_QS7_P	J26	PS_DDR_QS_P7_504	PS_DDR_DM6_504	L27 PS_DDR4_DM6	>> PS_DDR4_DM5	13
14 PS_DDR4_QS7_N	PS_DDR4_QS7_N	J27	PS_DDR_QS_N7_504	PS_DDR_DM7_504	H26 PS_DDR4_DM7	>> PS_DDR4_DM7	13
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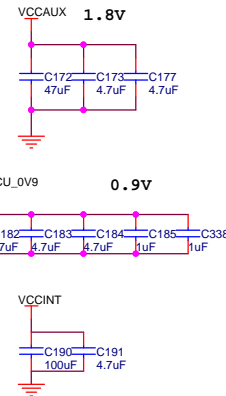
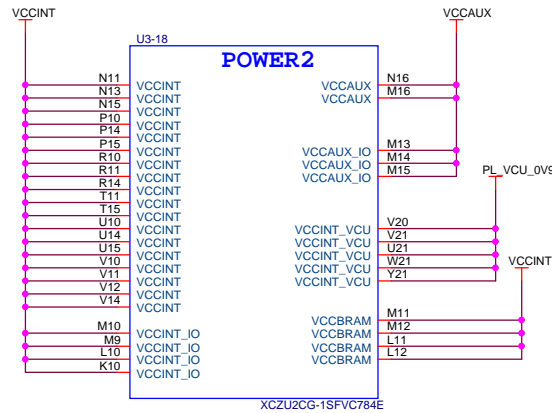
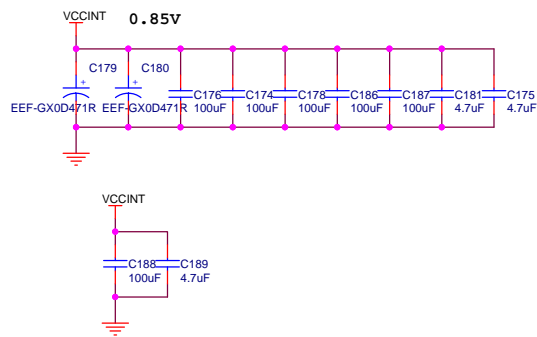
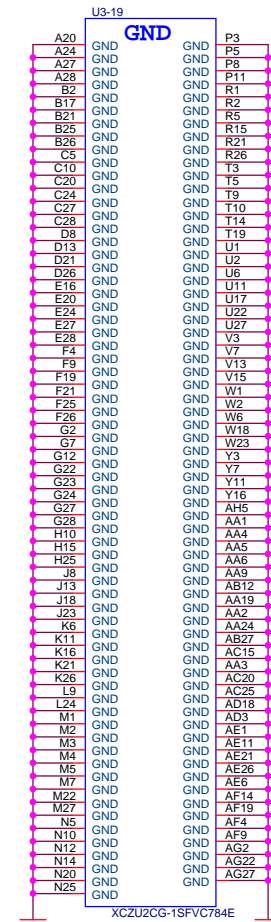
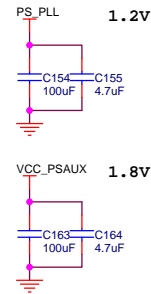
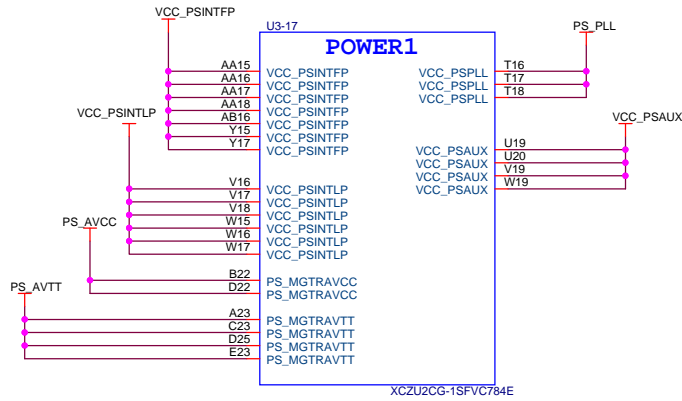
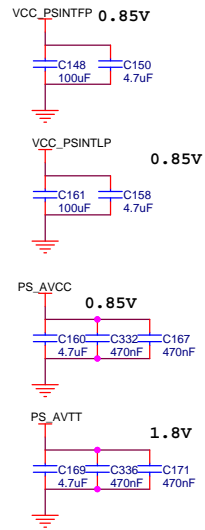
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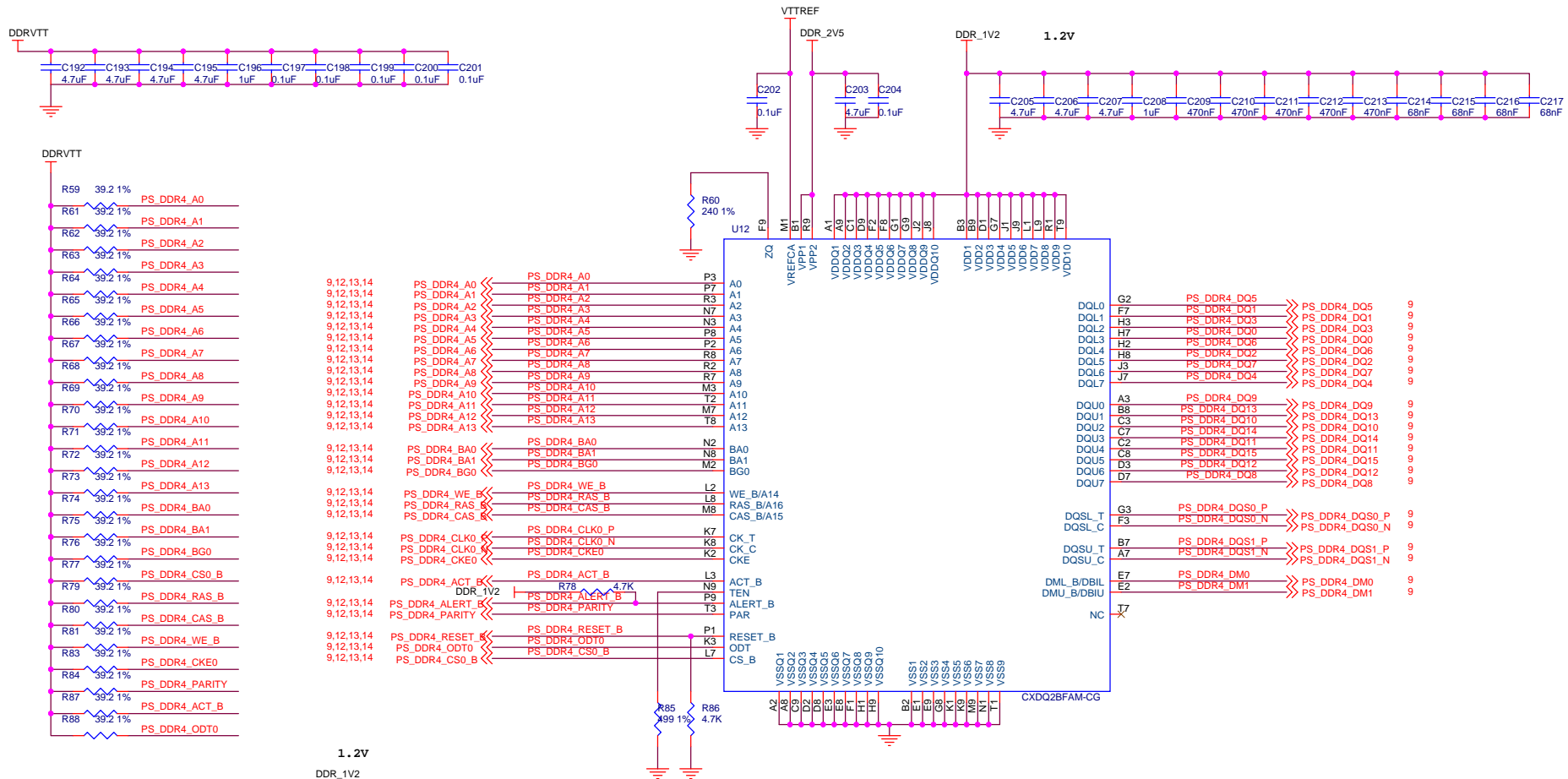
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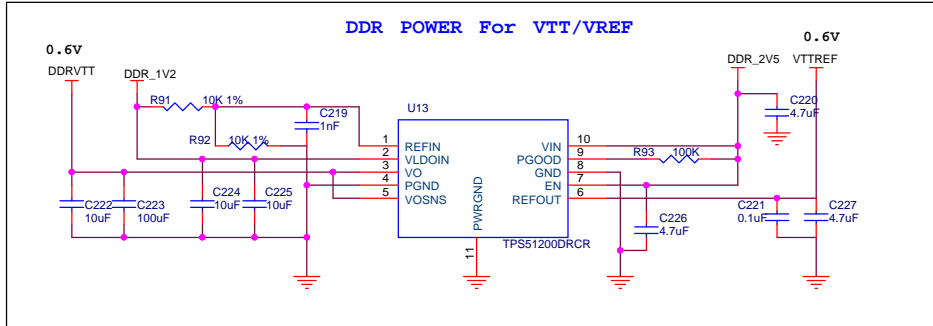
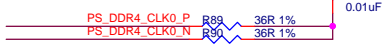
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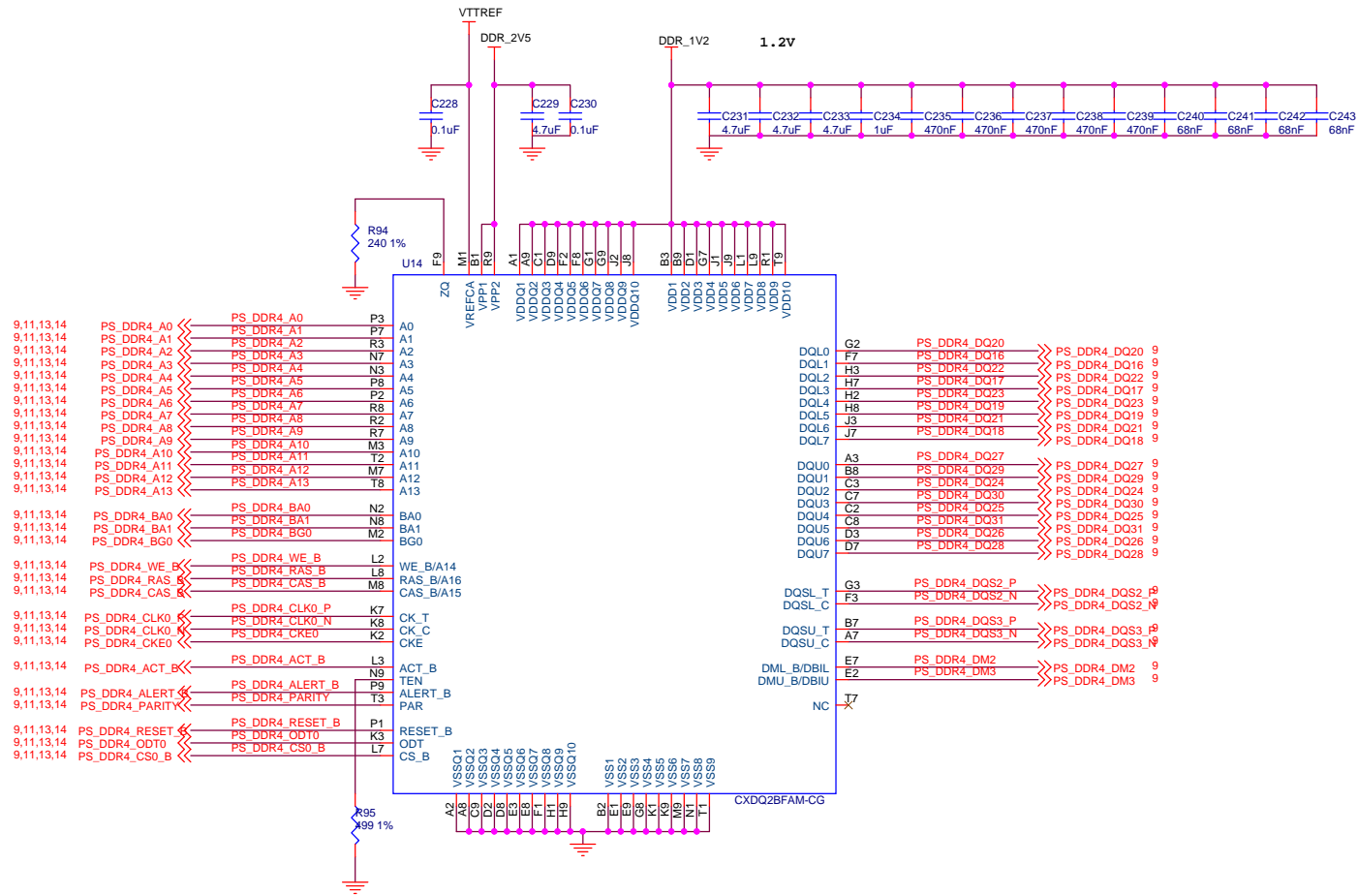
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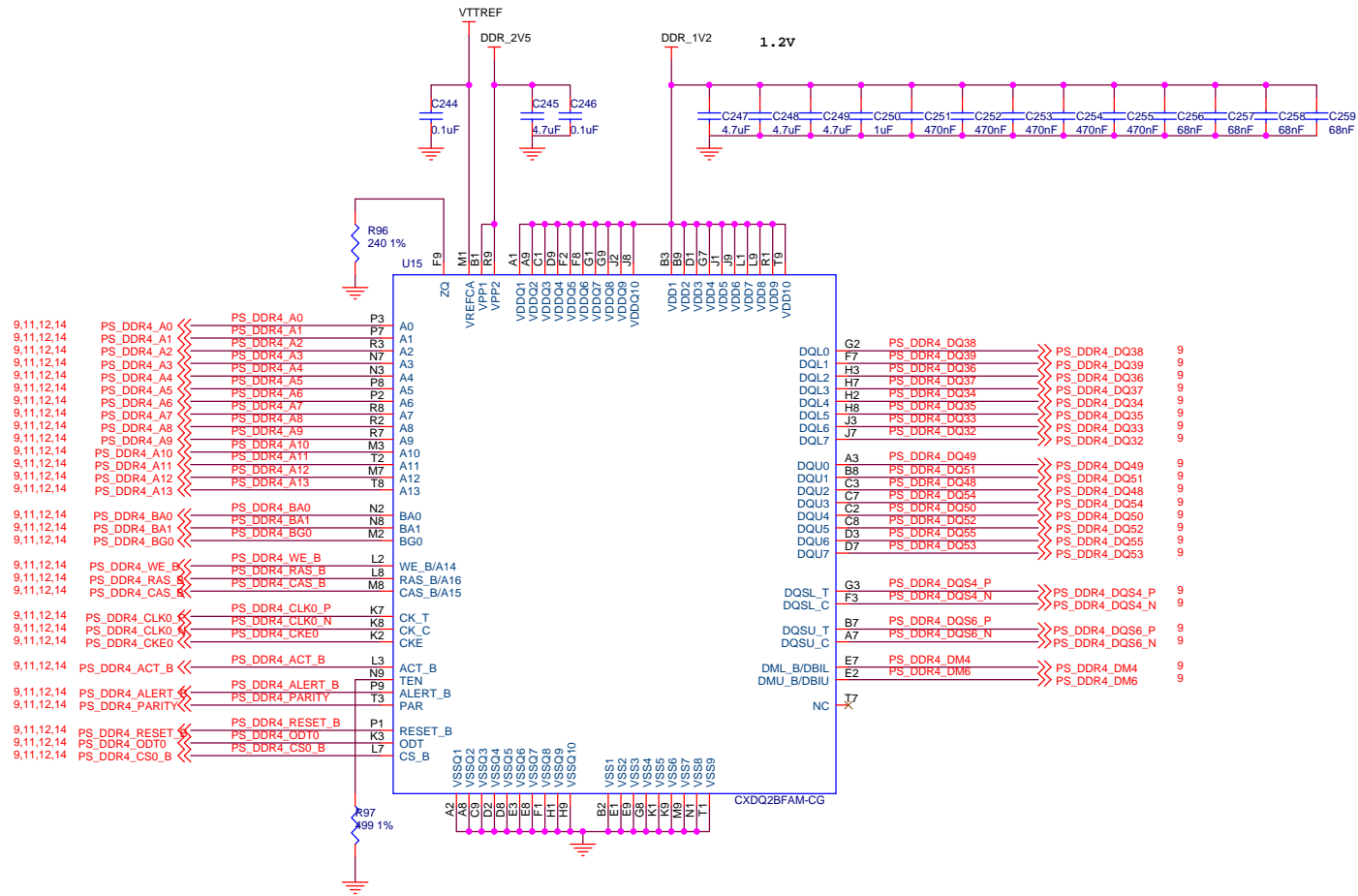


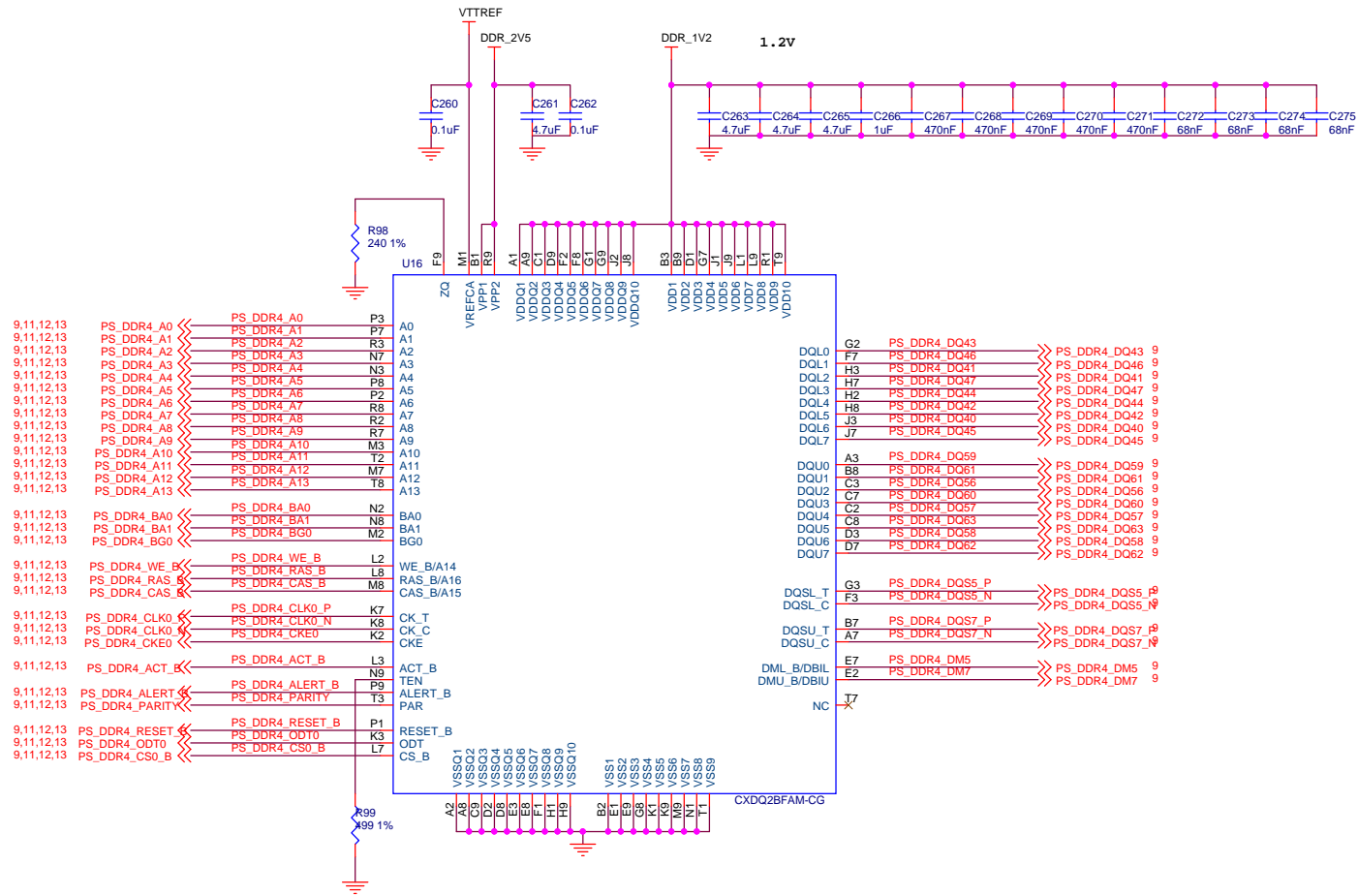


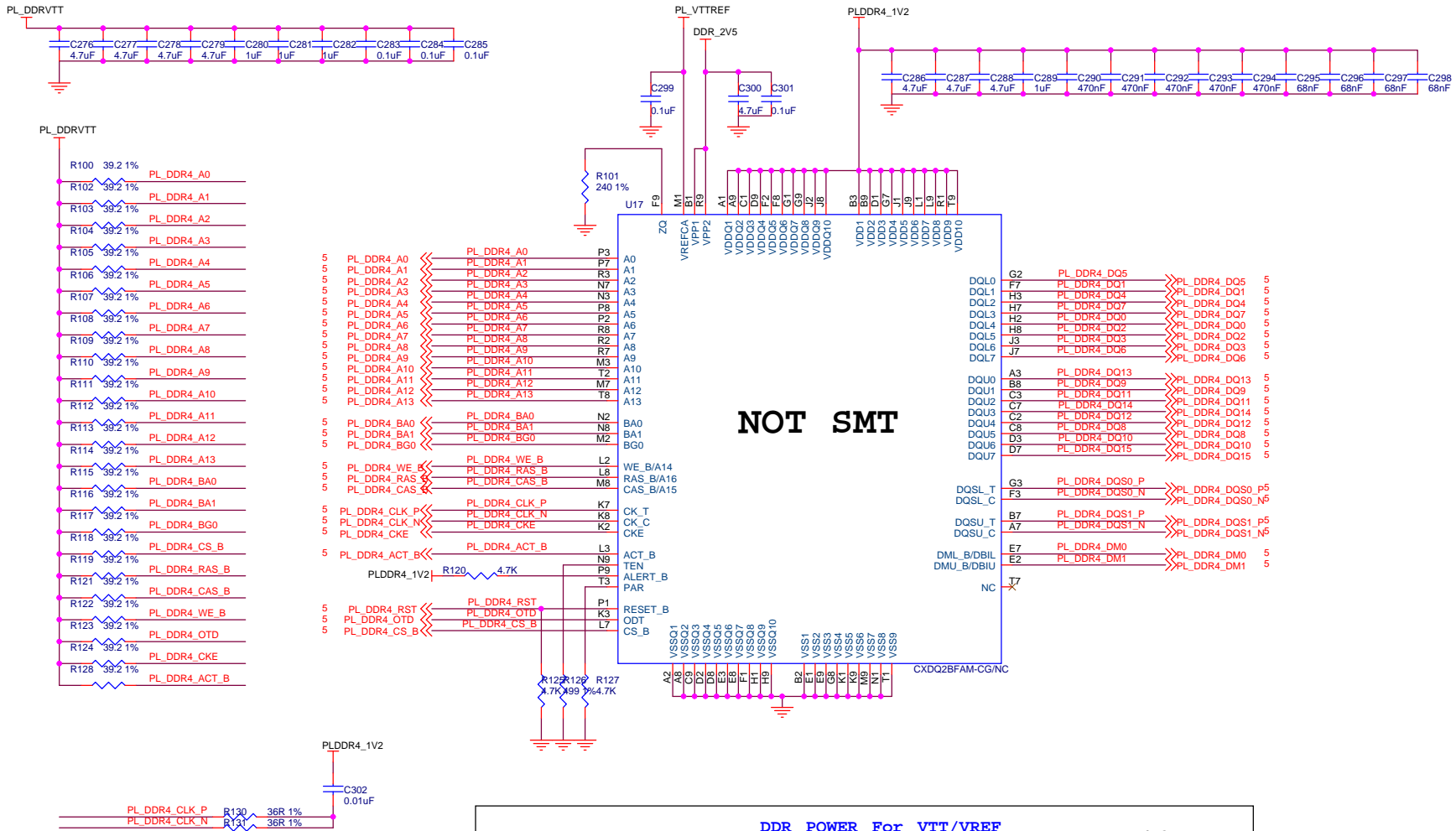
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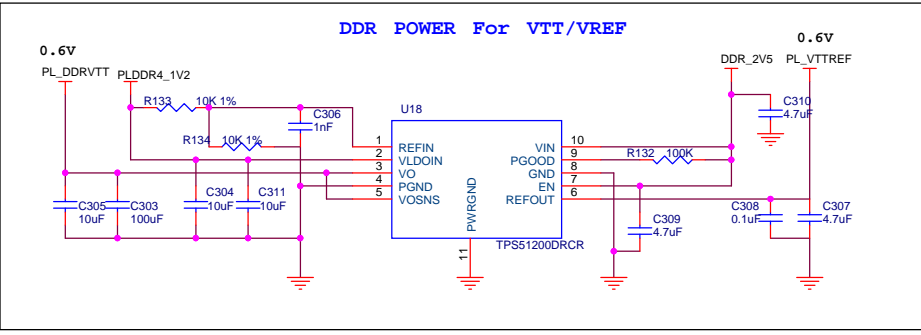


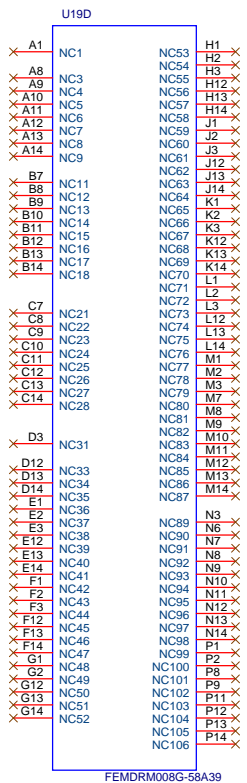




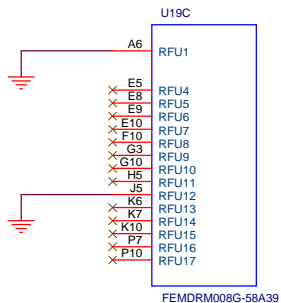


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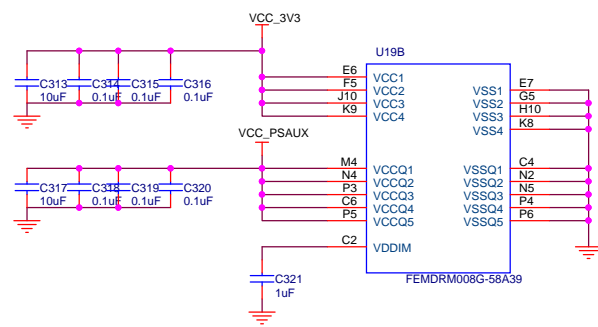
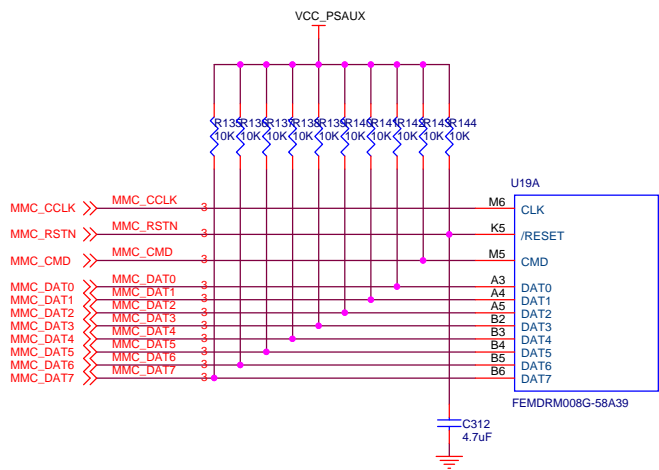




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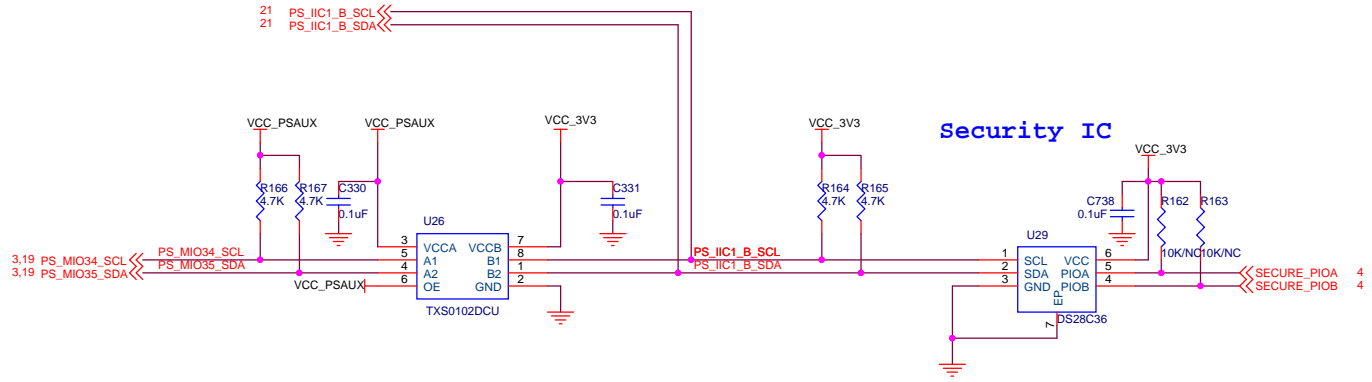
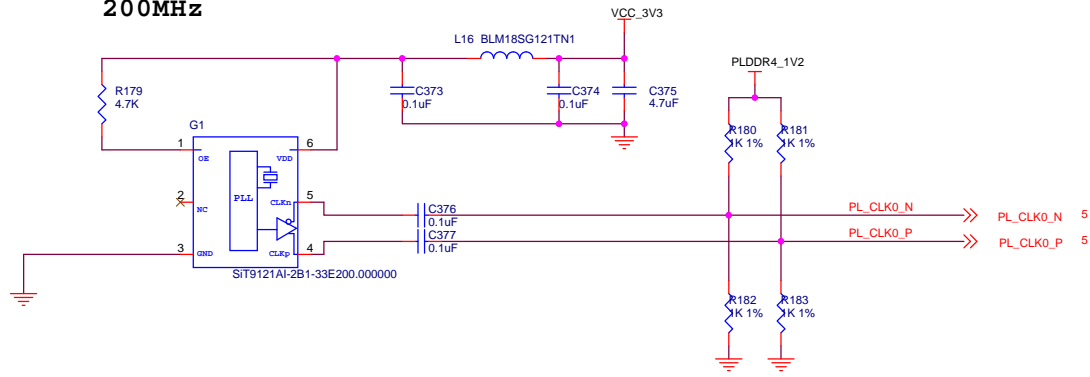


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PL SYSTEM CLOCK

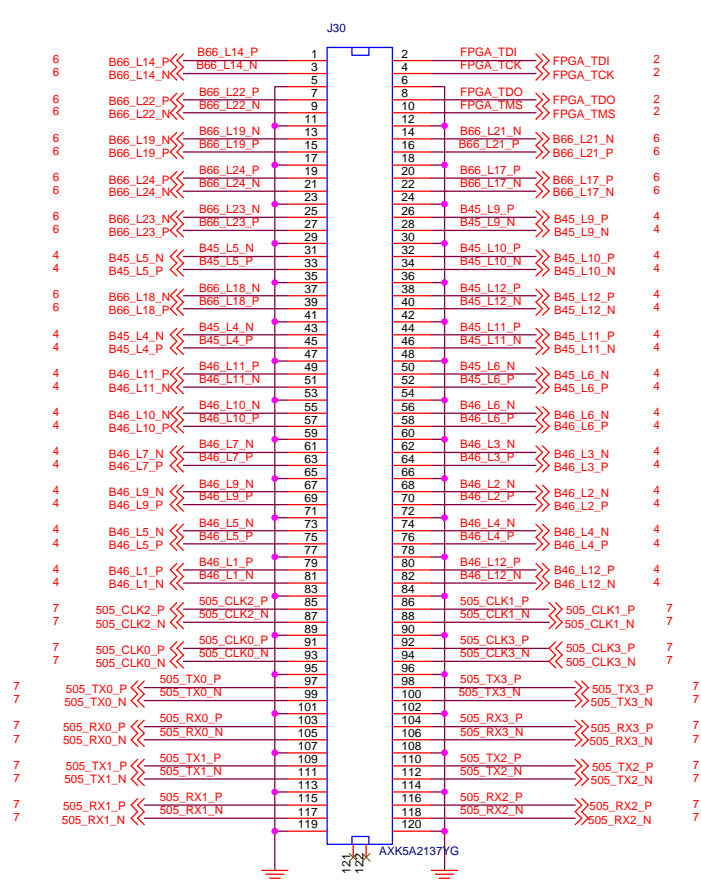
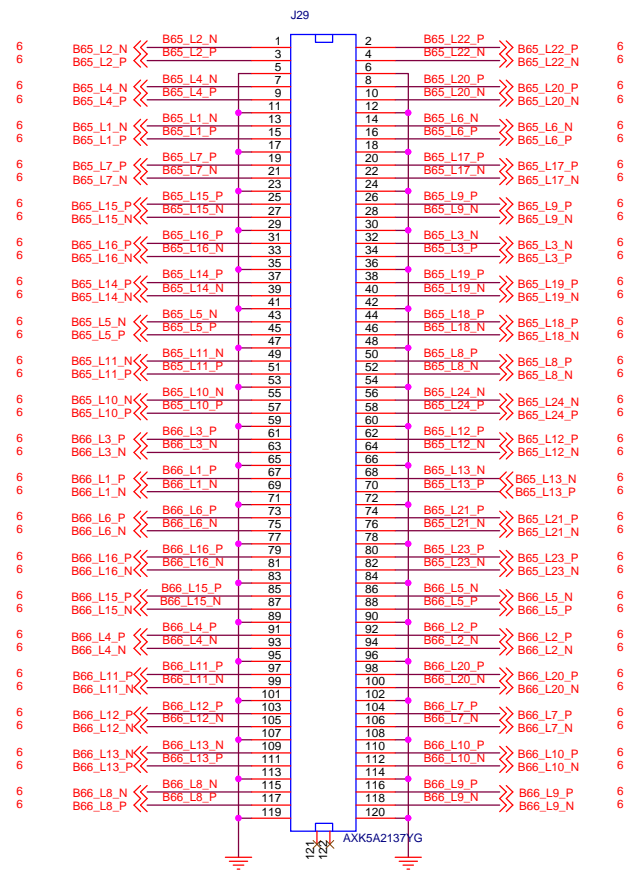
200MHz



PS_IIC1: IIC ADDRESS IS 0x1B

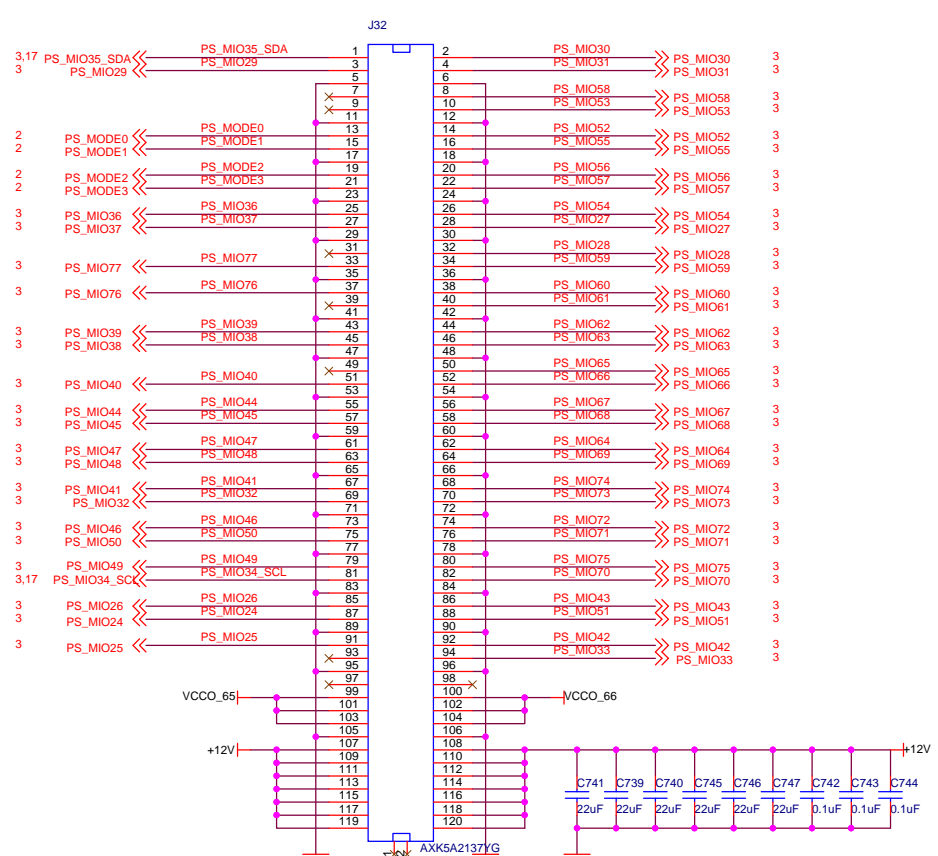
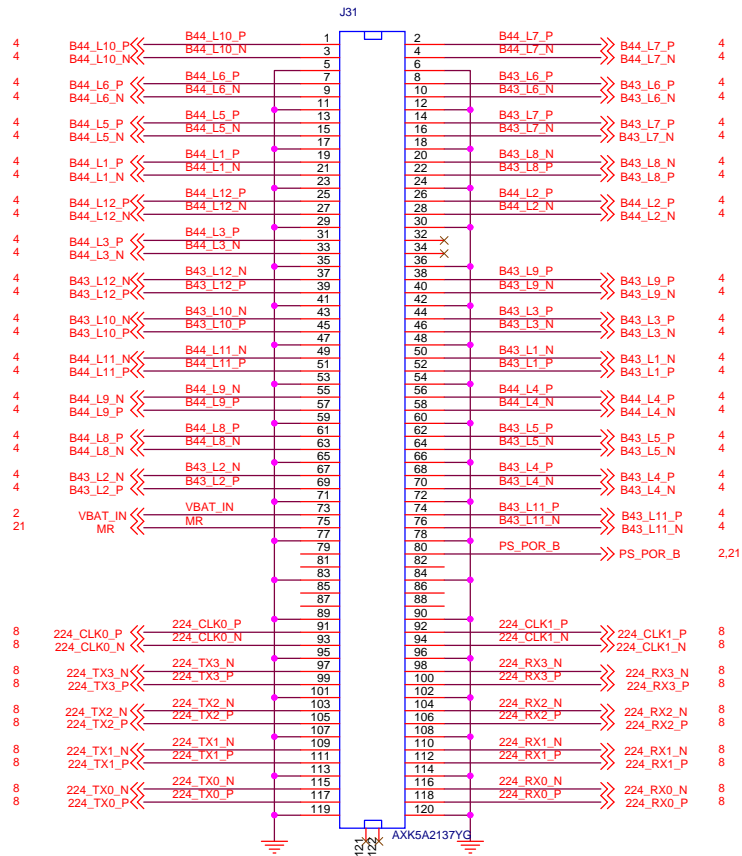
BANK65, BANK66 IO Voltage can not exceed +1.8V

BANK45, BANK46 IO Voltage is +3.3V Standard



BANK43, BANK44 IO Voltage is +3.3V Standard

The MIO Voltage is +1.8V Standard

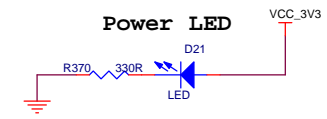
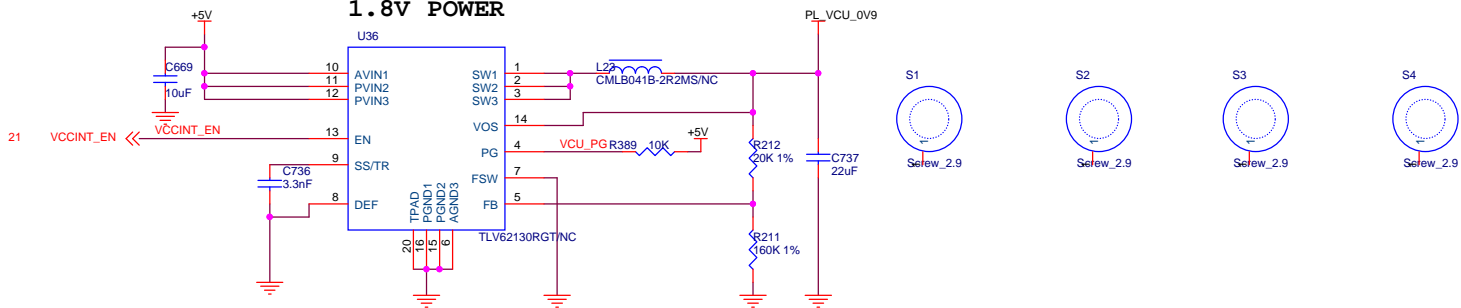


VCCO_65 VCCO_66 Power supply can not exceed 1.8V

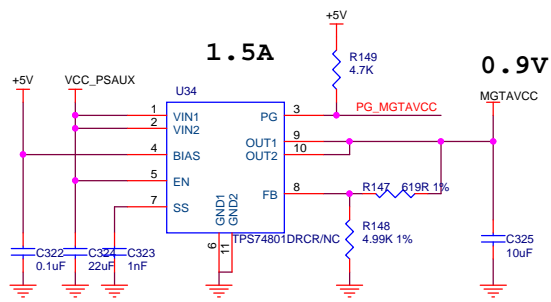
POWER ON: VCCINT/VCCINT_IO/VCCBRAM(+0.85V)->VCCINT_VCU(+0.9V)->VCCAUX/VCCAUX_IO(+1.8V)->VCCO(+3.3V, +1.8V)

POWER ON: VCCINT(+0.85V)->MGTAVCC(+0.9V)->MGTAVTT(+1.2V)

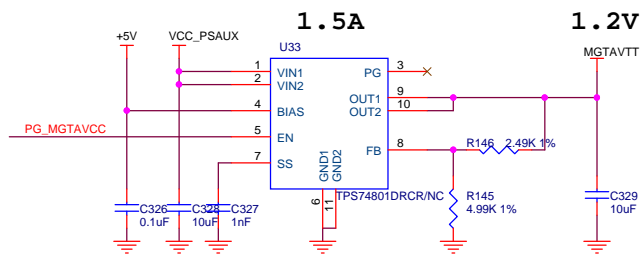
1.8V POWER



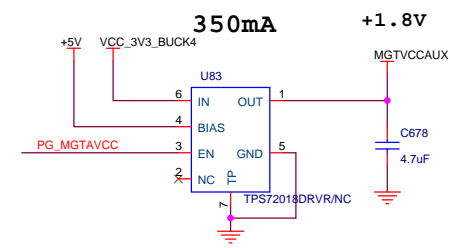
1.5A



1.5A

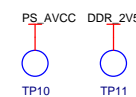
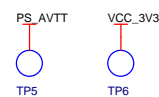
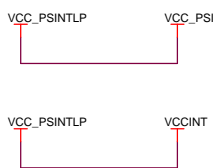
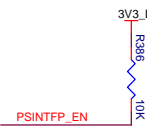
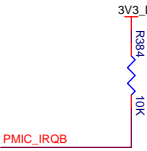
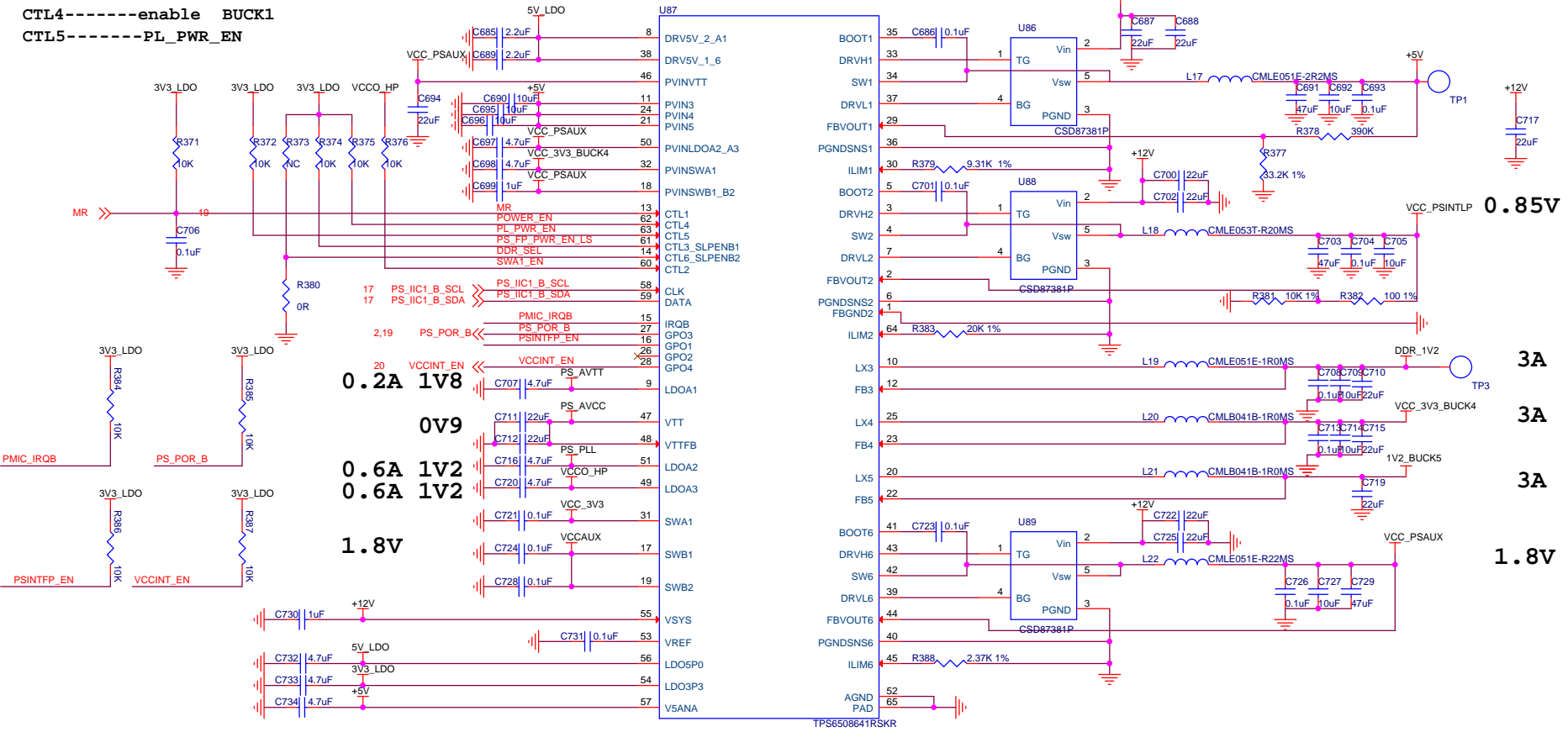


350mA



GPO1-----BUCK1_2_PG
GPO4-----BUCK4_PG

CTL2-----enable and disable SWA1
CTL3-----PS_FP_PWR_EN_LS
CTL4-----enable BUCK1
CTL5-----PL_PWR_EN



PS_IIC0: IIC ADDRESS IS 0x5E